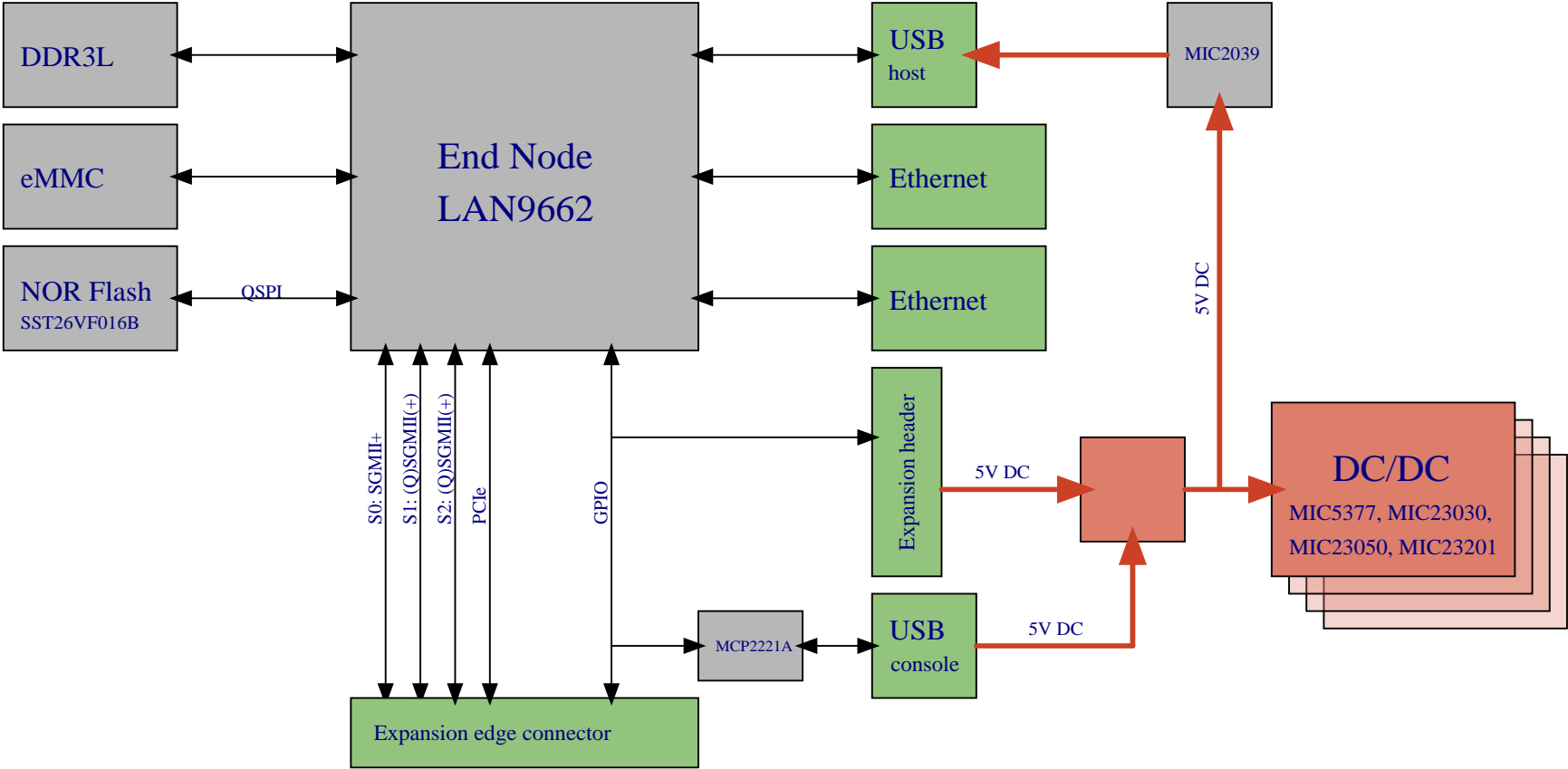


LAN9662 End Node module

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3	LAN9662 DDR
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5	Expansion connector & USB
6	Power Supplies

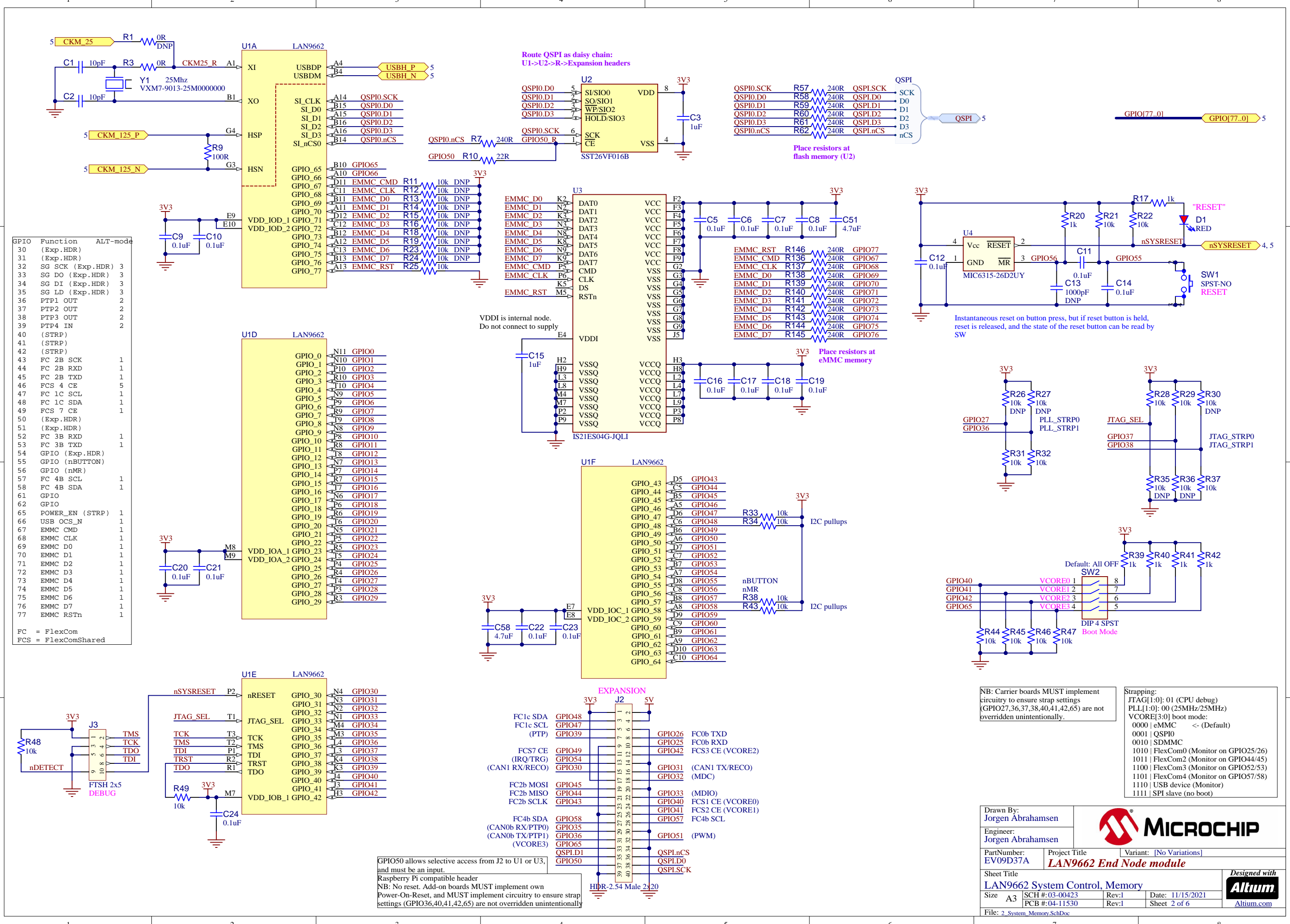


Design Defaults

Resistors are 1% tolerance.
Signals are nominal 50 Ohms.

Revision History

Revision	Date	Revision Summary	Author
B0	2021/03/25	Update edge connector footprint	Jorgen Abrahamsen
1	2021/10/19	Fix VPH_PCIE. BOM optimizations	Jorgen Abrahamsen





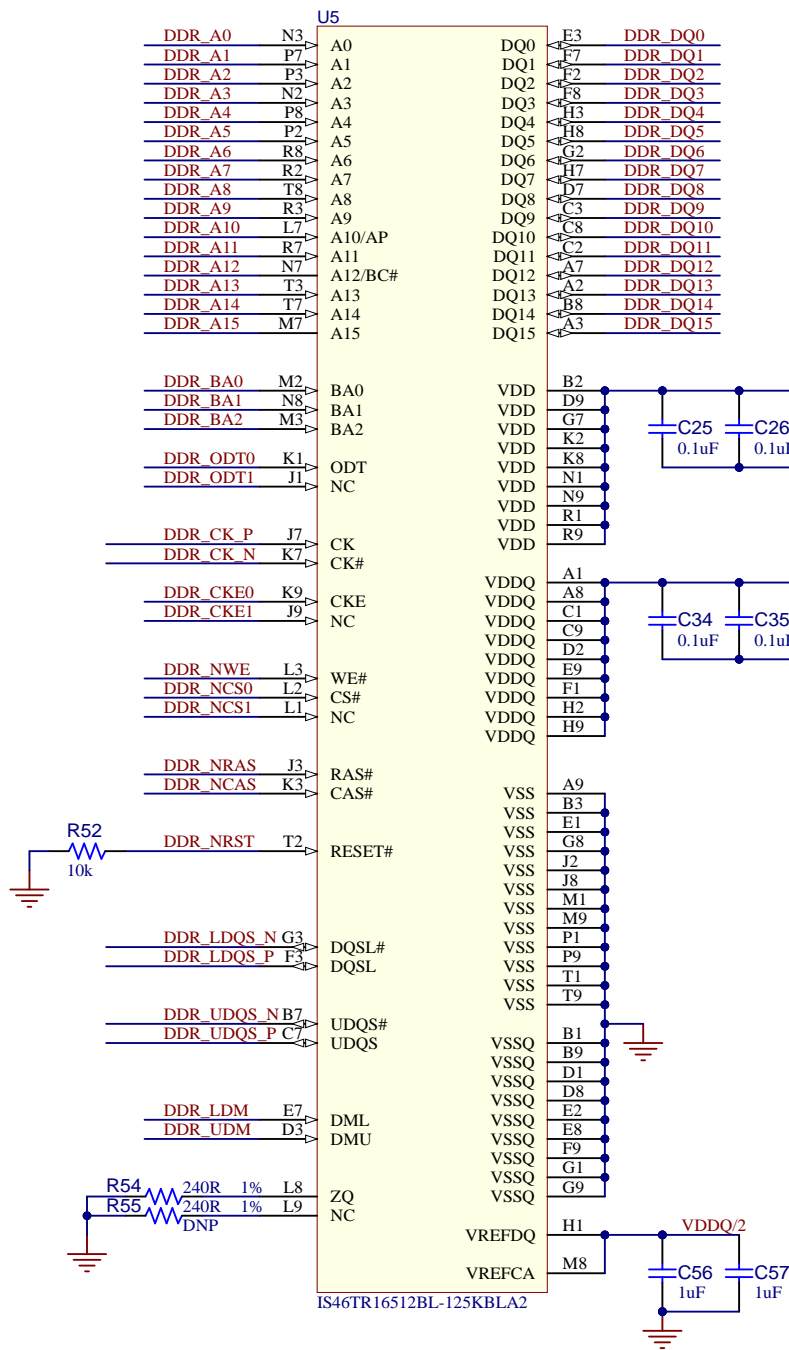
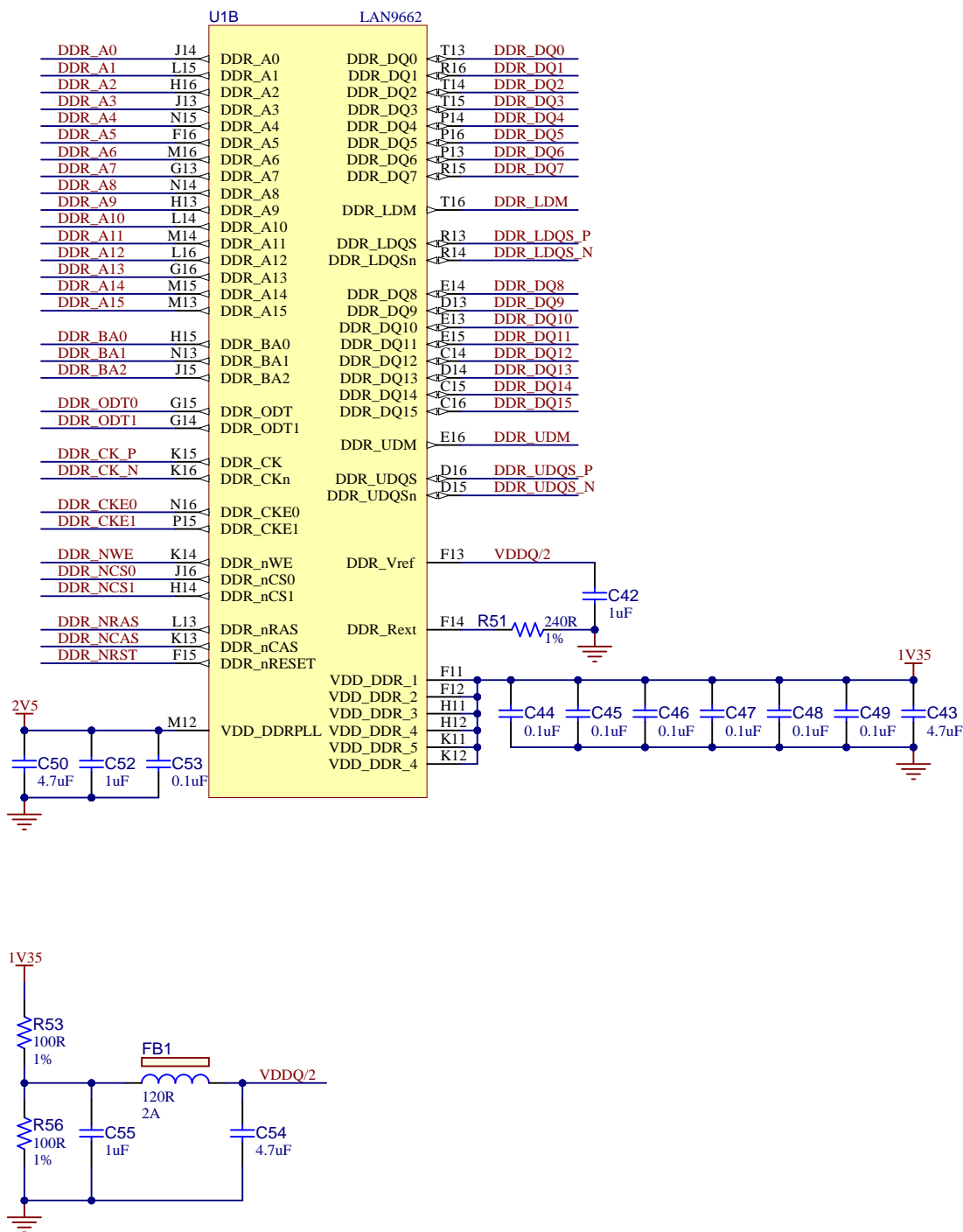
GPIO	Function	ALT-mode
30	(Exp.HDR)	
31	(Exp.HDR)	
32	SG SCK (Exp.HDR)	3
33	SG DO (Exp.HDR)	3
34	SG DI (Exp.HDR)	3
35	SG LD (Exp.HDR)	3
36	PTP1 OUT	2
37	PTP2 OUT	2
38	PTP3 OUT	2
39	PTP4 IN	2
40	(STRP)	
41	(STRP)	
42	(STRP)	
43	FC 2B SCK	1
44	FC 2B RXD	1
45	FC 2B TXD	1
46	FCS 4 CE	5
47	FC 1C SCL	1
48	FC 1C SDA	1
49	FCS 7 CE	1
50	(Exp.HDR)	
51	(Exp.HDR)	
52	FC 3B RXD	1
53	FC 3B TXD	1
54	GPIO (Exp.HDR)	
55	GPIO (nBUTTON)	
56	GPIO (nMR)	
57	FC 4B SCL	1
58	FC 4B SDA	1
61	GPIO	
62	GPIO	
65	POWER_EN (STRP)	1
66	USB OCS_N	1
67	EMMC CMD	1
68	EMMC CLK	1
69	EMMC D0	1
70	EMMC D1	1
71	EMMC D2	1
72	EMMC D3	1
73	EMMC D4	1
74	EMMC D5	1
75	EMMC D6	1
76	EMMC D7	1
77	EMMC RSTn	1

FC = FlexCom
FCS = FlexComShared

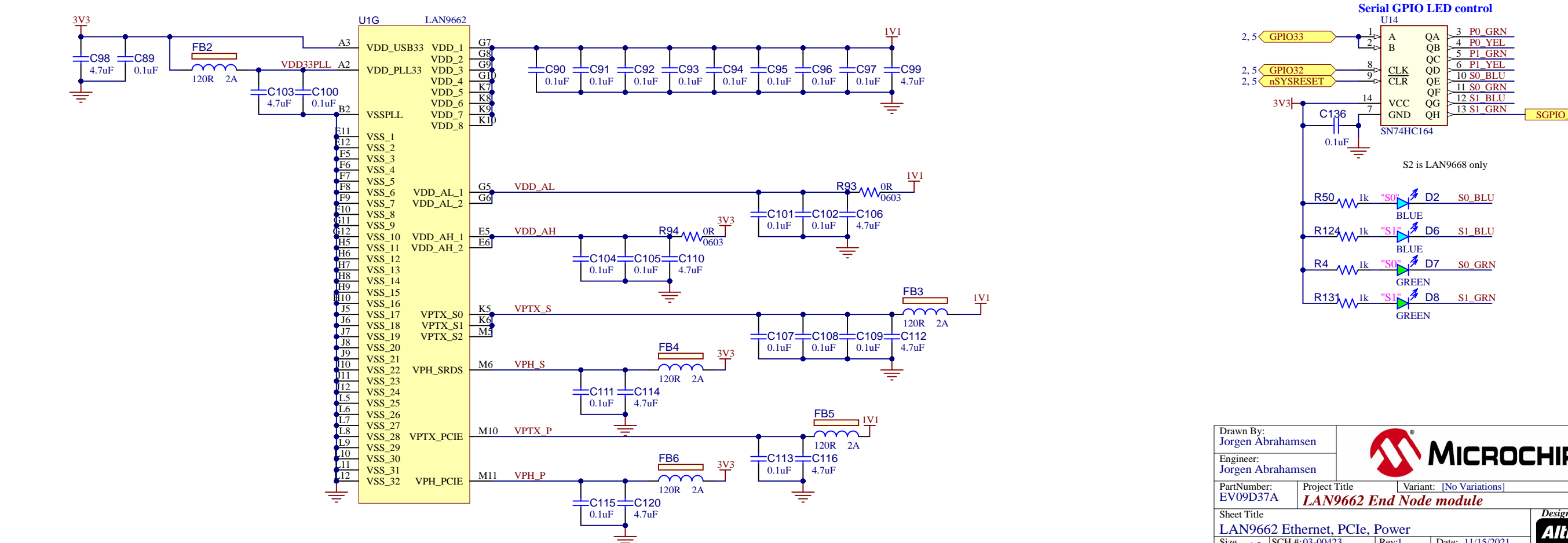
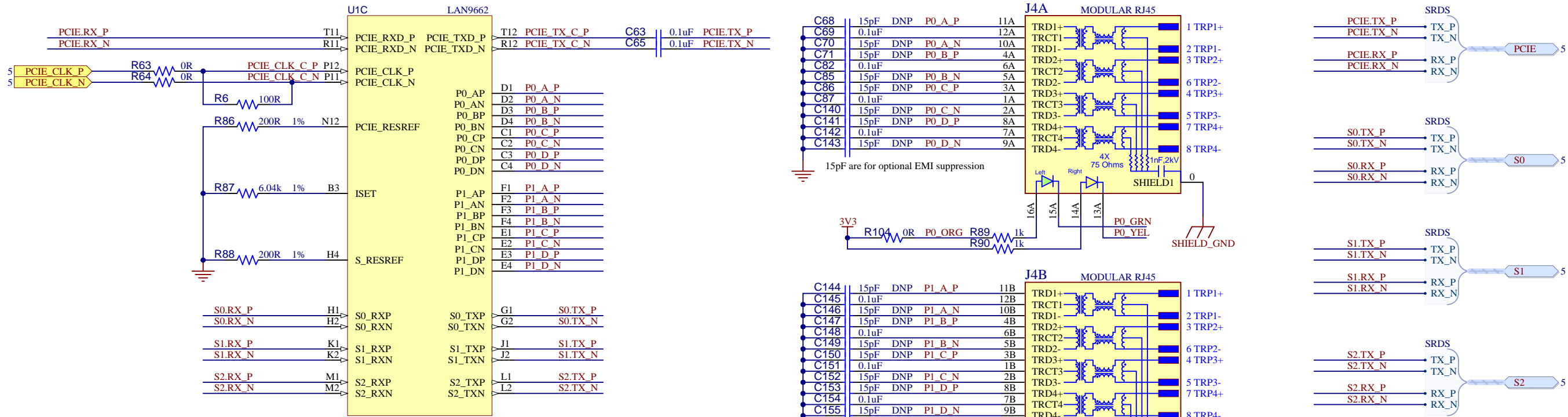
NB: Carrier boards MUST implement circuitry to ensure strap settings (GPIO27,36,37,38,40,41,42,65) are not overridden unintentionally.

Strapping:
JTAG[1:0]: 01 (CPU debug)
PLL[1:0]: 00 (25MHz/25MHz)
VCORE[3:0] boot mode:
0000 | eMMC <- (Default)
0001 | QSPI0
0010 | SDMMC
1010 | FlexCom0 (Monitor on GPIO25/26)
1011 | FlexCom2 (Monitor on GPIO44/45)
1100 | FlexCom3 (Monitor on GPIO52/53)
1101 | FlexCom4 (Monitor on GPIO57/58)
1110 | USB device (Monitor)
1111 | SPI slave (no boot)

Drawn By: Jorgen Abrahamsen			
Engineer: Jorgen Abrahamsen			
PartNumber: EV09D37A	Project Title LAN9662 End Node module	Variant: [No Variations]	
Sheet Title LAN9662 System Control, Memory			
Size A3	SCH #:03-00423	Rev:l	Date: 11/15/2021
File: 2_System_Memory.SchDoc	PCB #:04-11530	Rev:l	Sheet 2 of 6
			Designed with  Altium.com



Design is prepared for dual-rank devices:
CKE1/ODT1/nCS1 are connected.



D

Power source switch:
When 5V supply on
expansion connectors is
higher than the %V_USB
supply, the 5V_USB
supply is disconnected.

Power supplies, worst case currents:
1.10V@1.4A: LAN9668 (1.2A/1.4A)
1.35V@0.4A: DDR (175mA), RAM (220mA)
2.50V@0.1A: DDR PLL (40mA)
3.30V@0.6A: LAN9668 (0.1A/0.3A), misc (0.3A)

Total standalone, incl conversion loss: 3.8W 5V@0.75A
Total on carrier, incl conversion loss: 4.8W 5V@1.0A

Sequencing: 1V1 -> 1V35/3V3

Place TPs at 2.54mm pitch.

All switching regulators:
Datasheet PCB layout
recommendations MUST be followed

Test points:
GND test pads must be placed 2.5mm
from corresponding power test pad

LABEL1

Product number/revision
Serial number

PCBA LABEL 18X6mm

PAD1 PAD2 PAD3 PAD4

Rubber Pad Cyl D7.9H5.3

Pads in corners

Fiducials

FD1 FIDUCIAL
FD2 FIDUCIAL
FD3 FIDUCIAL
FD4 FIDUCIAL
FD5 FIDUCIAL
FD6 FIDUCIAL

Mounting Holes

MH1 MH2 MH3 MH4
Mounting holes in corners

Drawn By:
Jorgen Abrahamsen
Engineer:
Jorgen Abrahamsen



PartNumber: EV09D37A Project Title: LAN9662 End Node module Variant: [No Variations]

Sheet Title: Power Supplies
Size: A3 SCH #:03-00423 Rev:l Date: 11/15/2021
PCB #:04-11530 Rev:l Sheet 6 of 6

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