



# **EVB-LAN9662-NIC**

## **User's Guide**

Network Interface Card for LAN9662

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## Preface

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### NOTICE TO CUSTOMERS

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Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXA”, where “XXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

## INTRODUCTION

This chapter contains general information that will be useful to know before using the Microchip EVB-LAN9662-NIC Evaluation Board. Items discussed in this chapter include:

- [Document Layout](#)
- [Conventions Used in this Guide](#)
- [The Microchip Website](#)
- [Development Systems Customer Change Notification Service](#)
- [Customer Support](#)
- [Document Revision History](#)

## DOCUMENT LAYOUT

This document features the EVB-LAN9662-NIC Evaluation Board. The manual layout is as follows:

- **Chapter 1. “Overview”** – This chapter provides a brief overview of the EVB-LAN9662-NIC board and its features.
- **Chapter 2. “Management Software”** – This chapter provides information on the software management of the EVB-LAN9662-NIC.
- **Chapter 3. “EVB-LAN9662-NIC Overview”** – This chapter gives a quick overview of the EVB-LAN9662-NIC features.
- **Chapter 4. “EVB-LAN9662-NIC Hardware Details”** – This chapter provides hardware details of the EVB-LAN9662-NIC PCB.
- **Appendix A. “PCB Layout and Silk Screens”** – This appendix shows the PCB layout images of EVB-LAN9662-NIC.

## CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

### DOCUMENTATION CONVENTIONS

Description	Represents	Examples
<b>Arial font:</b>		
Italic characters	Referenced books	<i>MPLAB® IDE User's Guide</i>
	Emphasized text	...is the <i>only</i> compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	<u><i>File&gt;Save</i></u>
Bold characters	A dialog button	Click <b>OK</b>
	A tab	Click the <b>Power</b> tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
<b>Courier New font:</b>		
Plain Courier New	Sample source code	#define START
	Filenames	autoexec.bat
	File paths	c:\mcc18\h
	Keywords	_asm, _endasm, static
	Command-line options	-Opa+, -Opa-
	Bit values	0, 1
	Constants	0xFF, 'A'
Italic Courier New	A variable argument	<i>file.o</i> , where <i>file</i> can be any valid filename
Square brackets [ ]	Optional arguments	mcc18 [options] file [options]
Curly brackets and pipe character: {   }	Choice of mutually exclusive arguments; an OR selection	errorlevel {0 1}
Ellipses...	Replaces repeated text	var_name [, var_name...]
	Represents code supplied by user	void main (void) { ... }

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- **Emulators** – The latest information on Microchip in-circuit emulators. This includes the MPLAB® REAL ICE™ and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICKit™ 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are non-production development programmers such as PICSTART® Plus and PICKit™ 2 and 3.

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- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

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Technical support is available through the website at:

<http://www.microchip.com/support>

## DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50003439A (11-22-22)	Initial release	



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## Chapter 1. Overview

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### 1.1 INTRODUCTION

This hardware manual describes the design of the EVB-LAN9662-NIC network interface card, demonstrating the LAN9662 AVB/TSN Ethernet switch architecture with Real-Time Engine (RTE) functionality. The EVB-LAN9662-NIC is based on the EV53U25A-1 (UNG8314B) reference design.

This document is intended primarily hardware and software engineers who want to get an overview of designing products based on the LAN9662.

### 1.2 REFERENCES

Concepts and materials available in the following documents may be helpful when reading this document. Visit [www.microchip.com](http://www.microchip.com) for the latest documentation.

- *LAN9662 Data Sheet*
- *EV53U25A-1 Reference Design Schematic*
- BSP Documentation ([http://mscc-ent-open-source.s3-eu-west-1.amazonaws.com/public\\_root/bsp/mscc-brsdk-doc-2022.09.html](http://mscc-ent-open-source.s3-eu-west-1.amazonaws.com/public_root/bsp/mscc-brsdk-doc-2022.09.html))
- Linux Documentation
  - -Switchdev (<https://www.kernel.org/doc/html/latest/networking/switchdev.html>)
  - Traffic Control (<https://tldp.org/en/Traffic-Control-HOWTO>)

### 1.3 TERMS AND ABBREVIATIONS

The following are the terms and abbreviations used in this document:

- AMS – Automatic Media-Sense
- ANEG – Auto-negotiation
- CLI – Command Line Interface
- EMI – Electromagnetic Interference, emissions
- HAT – Hardware Attached on Top
- ICE – In-Circuit Emulator
- JTAG – Joint Test Access Group, IEEE1149
- LVDS – Low Voltage Differential Signaling
- LVTTL – Low Voltage TTL
- NIC – Network Interface Card
- PCS – Physical Coding Sublayer
- PHY – Physical Layer Device
- PTP – Precision Time Protocol, IEEE1588
- RTE – Real-Time Engine
- SFP – Small Form-Factor Pluggable
- SGMII – Serial Gigabit Media Independent Interface
- SI – Serial Interface, SPI
- SME – Small/Medium Enterprise

- SSM – Synchronization Status Message
- SyncE – Synchronous Ethernet, ITU-T G.8262/Y.1362

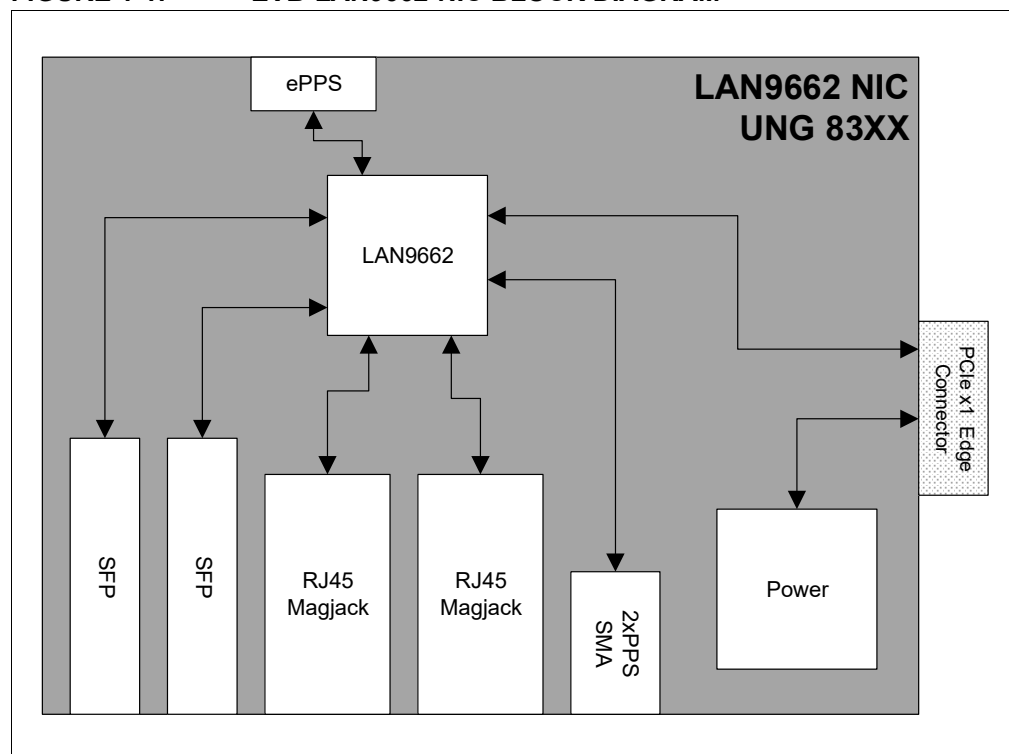
## 1.4 EVB-LAN9662-NIC OVERVIEW

The ATX-style EVB-LAN9662-NIC is a PC 4-port Ethernet network interface card (NIC) that uses LAN9662. It exposes the two integrated 10/100/1000BASE-T ports on LAN9662 and the two Gigabit Ethernet SFP ports. It connects to a PC using PCIe® 2.0. The internal ARM-based CPU system is not used in this application.

Figure 1-1 briefly shows the different interface types available on the EVB-LAN9662-NIC:

- Two SFP cages connected to LAN9662 internal SerDes ports
- Two tri-speed (10/100/1000BASE-T) RJ45 ports using the LAN9662 internal copper PHYs
- Two SMA connectors for PTP/IEEE1588v2 applications: 1PPS input and output SMAs
- ePPS intercard interconnect to synchronize multiple EVB-LAN9662-NICs in a PC
- PCIe x1 Edge connector

**FIGURE 1-1: EVB-LAN9662-NIC BLOCK DIAGRAM**



## 1.5 FEATURES

The EVB-LAN9662-NIC features:

- Interface
  - LEDs: Reset and port status
- Power supplies
  - 3.3V from PCIe Edge connector
  - Local supplies: 1.1V to LAN9662

- Connectors
  - Two RJ45 with integrated status LEDs
  - Two SFP connectors with associated status LEDs on PCB
  - 1PPS input (external SMA)
  - 1PPS output (internal SMA)
  - PCIe x1 Edge connector
  - 10-pins, 0.1" right-angle header for internal ePPS distribution
  - 10-pins, 0.1" straight header for QSPI1 access for possible RTE access
  - 40-pins, 0.1" Expansion header (RPI-compatible HAT) with SPI, I<sup>2</sup>C and UART (also used for NOR Flash programming)
- PCIe features
  - PCIe JTAG connection to LAN9662 (The LAN9662 JTAG can be disconnected and used for SW debug as a resistor mount option.)

## 1.6 MANAGEMENT

Management of the EVB-LAN9662-NIC requires basic Ethernet NIC drivers for Linux<sup>®</sup> (both ARM and x86 architectures) and for Windows<sup>®</sup>.

For Linux, the following additional functions are needed:

- SFP port and control
- PTP4L
- Switchdev
- End-node RTE functionality (PROFINET/OPC-UA)

## 1.7 NETWORK PORTS

The EVB-LAN9662-NIC offers two tri-speed Cu PHY ports, which have low EMI line drivers with integrated line-side termination resistors and support for HP Auto MDI-/MDI-X<sup>™</sup>. The PHY ports operate over standard Category 5 cabling at 10/100/1000 Mbit/s and Category 3 cabling at 10 Mbit/s.

The NIC card offers additional two SFP connectors supporting 100BASE-FX, 1000BASE-X with Clause 37 ANEG and 2.5GBASE-X Optical SFP modules, Cu SFP modules over SGMII with the Cisco-defined SGMII ANEG, or SFP DAC cabling for 2.5G SGMII+.

## 1.8 TIMING AND SYNCHRONIZATION

### 1.8.1 SyncE

SyncE is not supported on this evaluation platform.

### 1.8.2 PTP/IEEE1588v2/802.1AS-2020

PTP interfacing is available through all network ports with high accuracy timestamping in the LAN9662, through an ePPS header, and through input and output of 1PPS SMA connectors.

The LAN9662 can be configured as a boundary clock, transparent clock, PTP time-Transmitter, or PTP timeReceiver. LAN9662 supports both one-step and two-step operations. Multiple time domains are available.

NOTES:

## Chapter 2. Management Software

### 2.1 INTRODUCTION

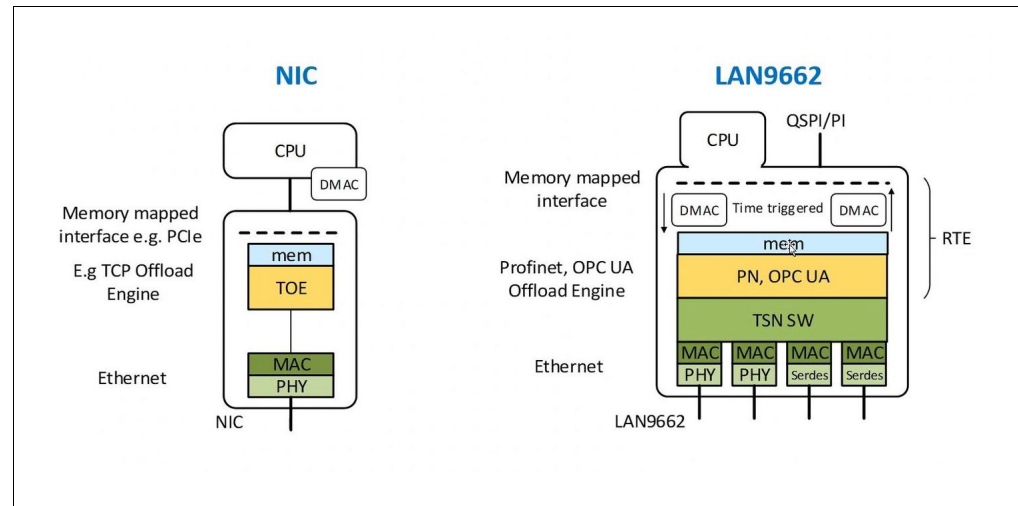
The EVB-LAN9662-NIC is managed through standard Linux commands. When connected, the desktop detects the NIC card on its PCIe root-complex.

### 2.2 SWITCHDEV DRIVER FOR MANAGEMENT

The Switchdev driver for LAN9662 is integrated into the Linux kernel, so that users will not detect if standard Linux software forwarding is used, or if the functionality is off-loaded by the LAN9662.

Figure 2-1 compares the EVB-LAN9662-NIC card to a standard Ethernet NIC card.

**FIGURE 2-1: EVB-LAN9662-NIC AND ETHERNET NIC COMPARISON**



The default startup mode is NIC functionality with no frame-forwarding. When bridges are added to the configuration, the Switchdev driver offloads the frame-forwarding to the LAN9662.

Most of the configuration is done using standard Linux commands from `iproute2` or the `libnl` libraries. Features not available in the upstream kernel are provided via extended features, which are non-upstream additions.

The tools supported in the Board Support Package (BSP) are shown in Table 2-1 and Table 2-2.

**TABLE 2-1: BSP SUPPORTED TOOLS**

Name	Origin	Example
Iproute2 Suite	Linux community	ip, bridge, tc
ethtool	Linux community	ethtool
ptp4l	Linux community	ptp4l
tiny-llpd	Linux community	tlldpd
QoS Tool	Microchip	qos

**TABLE 2-1: BSP SUPPORTED TOOLS (CONTINUED)**

Name	Origin	Example
VCAP Tool	Microchip	vcap
FP Tool	Microchip	fp
PSFP Tool	Microchip	psfp
FRER Tool	Microchip	frer

**TABLE 2-2: DEBUGGING TOOLS**

Name	Origin	Example
Debug Messages	Linux community	dmesg
Packet Capture	Linux community	tcpdump
Packet Injection/Capturing	Microchip	ef, ef-loop
ProcFS/DebugFS	Microchip	cat /proc/... cat /sys/kernel/info/...
Symbolic Register Access	Microchip	symreg

[Example 2-1](#) shows some examples of the Switchdev commands supported. Help is available through the normal Linux help commands.

**EXAMPLE 2-1: SWITCHDEV COMMANDS**

```
// Check link status
# ip -c link
// Set MAC address for port 0 and 1
# ip link set dev eth0 address 00:00:00:11:11:11
# ip link set dev eth1 address 00:00:00:22:22:22
// Set IP address
# ip address add dev eth0 192.168.1.1/24
// Enable port 0 and 1
# ip link set dev eth0 up
# ip link set dev eth1 up
// Show link details
# ip -d link show dev eth0
# ip -d link show dev eth1
// Show speed and duplex
# ethtool eth0
# ethtool eth1
// Setup a bridge to allow forwarding between port 0 and 1
# ip link add name br0 type bridge
# ip link set dev eth1 master br0
# ip link set dev eth0 master br0
// Check bridge link state
# bridge link show
// Enable VLAN awareness
# ip link set dev br0 type bridge vlan_filtering 1
// Check bridge VLAN state
# bridge vlan show
// Enable bridge 0
# ip link set dev br0 up
# bridge vlan show
// Check bridge link state
# bridge link show
// Show port statistics
# ip -s link show dev eth0
# ip -s link show dev eth1
```

For BSP and Linux documentation, see [Section 1.2 “References”](#).

## Chapter 3. EVB-LAN9662-NIC Overview

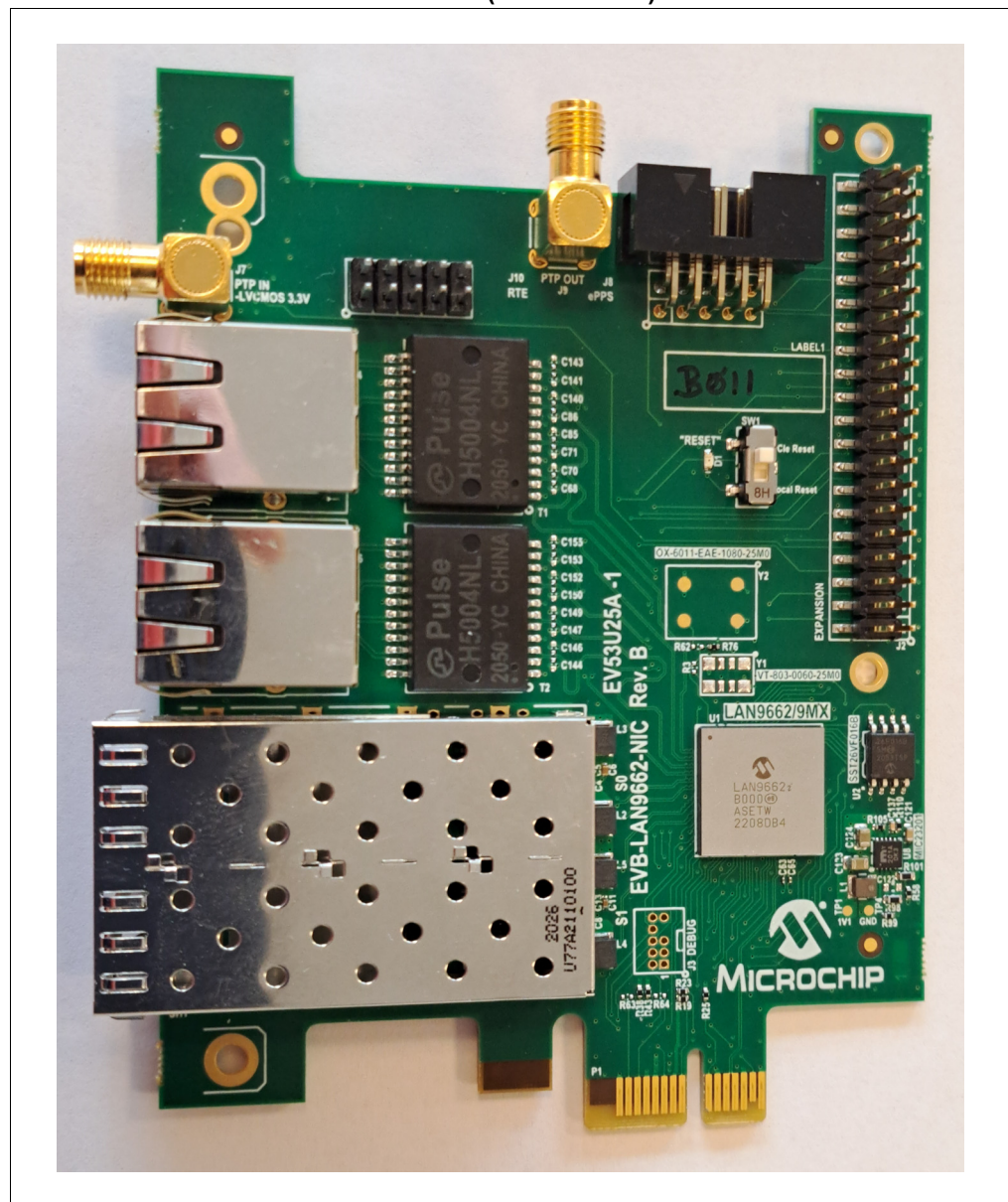
### 3.1 INTRODUCTION

This section gives an overview of the EVB-LAN9662-NIC.

### 3.2 BOARD OVERVIEW

Figure 3-1 shows the component placement on the EVB-LAN9662-NIC.

**FIGURE 3-1: EVB-LAN9662-NIC (REVISION B) BOARD**



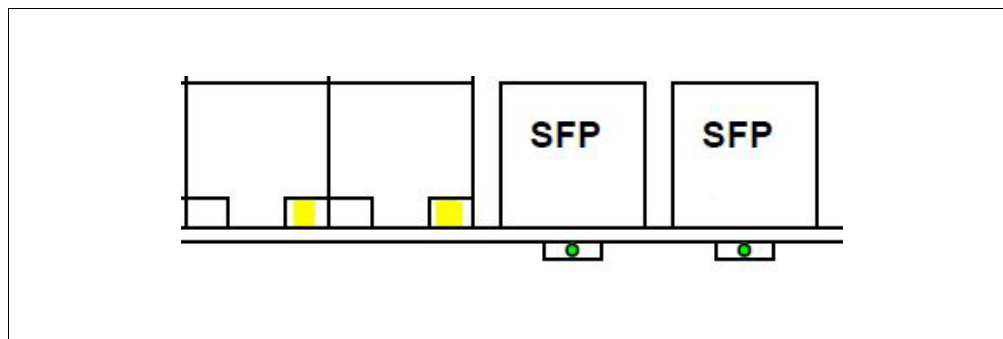
### 3.3 POWER

The EVB-LAN9662-NIC is powered through the PCIe Edge connector from the PC 3.3V power rail. An on-board DC/DC converter generates the 1.1V core supply needed for the LAN9662. The total power consumption, including conversion loss, is 5.0W.

### 3.4 FRONT PORT LAYOUT AND LEDS

Figure 3-2 shows the front port layout on the EVB-LAN9662-NIC.

**FIGURE 3-2: FRONT PORT LAYOUT ON EVB-LAN9662-NIC**



For each of the two copper ports, there are two LEDs (green/yellow) available in the RJ45 connector. Likewise, for the two SerDes ports, a bi-color LED (green/red) is placed underneath the PCB on each SFP cage.

### 3.5 SMA CONNECTORS

The EVB-LAN9662-NIC provides two SMA connectors for PTP applications.

One SMA connector is used as 1PPS output, J9, and is intended for system internal use. The output uses LVTTTL levels.

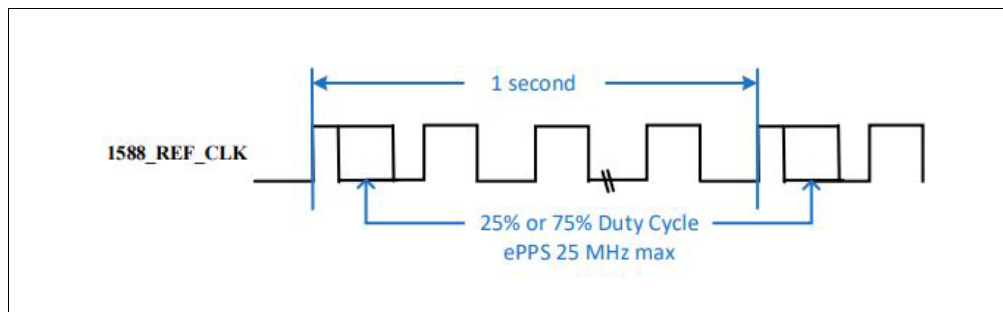
The other SMA connector is used as 1PPS input, J7, and is intended for external use. The input is LVTTTL and 3V3-tolerant.

### 3.6 ePPS HEADER

The ePPS header, J8, exposes three LAN9662 PTPSYNC (0-2) signals, which supports the ePPS format, where the 1PPS is combined with the 1588 clock. The clock can be 10 or 25 MHz. The ports can also be configured for 1PPS outputs or inputs.

The 1PPS pulse is coded into the 1588 clock signal by moving the falling edge of the clock signal at the appropriate time.

**FIGURE 3-3: ePPS CODING**





## 3.7 RTE HEADER

The LAN9662 RTE features can be explored using the RTE-associated control interface, QSPI1, which can be found in the RTE header, J10. The header is intended for system internal use. Likewise, two input/output (I/O) configurable (RTE) triggers can be found in this header.

## 3.8 EXPANSION HEADER (HAT)

The 2x10, 0.1" pin Expansion header targets Raspberry PI compatibility. It can also give an external CPU control over the SPI client register access interface or be used for programming the on-board NOR Flash device.

The Expansion header exposes various GPIO signals in the Alternate mode:

- UART: RXD, TXD (FLEXCOM 3b)
- I<sup>2</sup>C: SCL, SDA (FLEXCOM 1c)
- I<sup>2</sup>C: SCL, SDA (FLEXCOM 4b)
- SPI: SCLK, MISO, MOSI + Flex\_Shared 1/2 nCS (FLEXCOM 2b)
- QSPI0.SCK, QSPI0.D1, QSPI0.D0 and QSPI0.nCS (NOR Flash device or LAN9662)

The remaining Expansion header GPIO signals can function as normal GPIO pins when using default software settings. However, they can also be enabled with LAN9662-specific functionality, which is not found in the originally Raspberry PI header.

- CAN 0
- IRQ or TRG
- PWM
- PTP 0, 1, 2, 4
- Reset

Likewise, the on-board boot mode strapping, **VCORE\_CFG[3:0]**, can be overruled through this Expansion header.

**Note:** On the EVB-LAN9662-NIC, the Expansion header only provides 3.3V and not 5V.

## 3.9 PCIe<sup>®</sup> 1X EDGE CONNECTOR

The PCIe Edge connector gives an external CPU system access to the switch core register interface using the LAN9662 PCIe endpoint controller.

Likewise, the PCIe JTAG bus is connected to the LAN9662 JTAG.

## 3.10 DEBUG HEADER (OPTIONAL)

The EVB-LAN9662-NIC optionally provides a standard 10-pin (0.05") ARM CPU JTAG header, J3 (not mounted), to be used for In-Circuit Emulator (ICE). ICE can be used for debugging functions, such as downloading code and single-stepping through programs.

## 3.11 DEFAULT BOOT MODES AND REFERENCE CLOCK

The EVB-LAN9662-NIC is by default set to '0110' to support register setup from a PCIe host system.

The EVB-LAN9662-NIC supports a single 25 MHz clock source from either an XTAL or OSC.

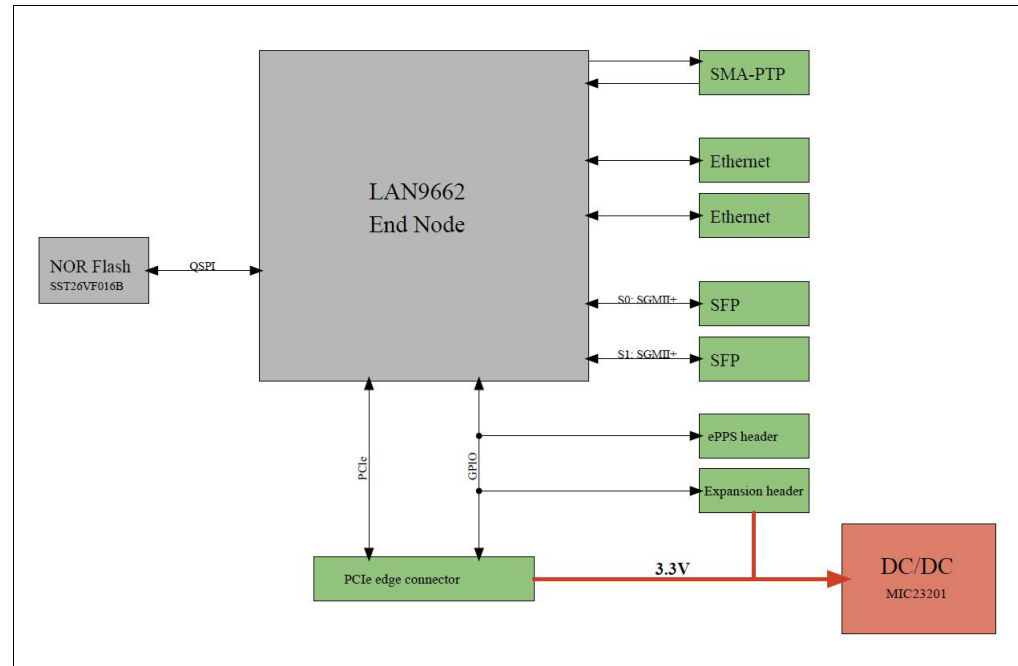
NOTES:

## Chapter 4. EV53U25A-1 Hardware Details

### 4.1 BLOCK DIAGRAM

Figure 4-1 depicts the block diagram of the EV53U25A-1 reference design used for the EV53U25A-1. The diagram shows the different interface types (in green) supported by LAN9662, and the on-board DC/DC converter (in red).

**FIGURE 4-1: EV53U25A-1 BLOCK DIAGRAM**



The following MCHP components are used (all active components on the board):

- One LAN9662
- One SST26VF016B NOR Flash device (optional)
- One MIC23201 DC/DC converter
- One VXM7-9013-25M0000000 XTAL

#### 4.1.1 Boot Mode Strapping

LAN9662 uses strapping pins to select the initial boot mode. These pins are named **VCORE\_CFG[3:0]** and are located on **GPIO[65,42,41,40]**. Resistors are used to make the actual strapping.

By default, the LAN9662 switch core is set up to be managed through its PCIe endpoint interface, but the strapping can also support other boot modes.

Alternatively, an external CPU can perform register access through the SPI client interface found in the Expansion header.

**Note:** When using QSPI0 as SPI client, the GPIO50 pin must also be pulled high in order not to chip-select the optional NOR Flash device. GPIO50 is also found in the Expansion header.

Table 4-1 shows the different boot modes supported from the NIC card.

**TABLE 4-1: EVB-LAN9662-NIC BOOT MODES SUPPORTED**

VCORE_CFG[3:0]	Description
0001	Boot from QSPI0 from the on-board Flash device (With boot traces on UART FLEXCOM 3b)
1000	TF-A monitor on UART FLEXCOM 3b
0110	Internal CPU is disabled. PCIe 2.0 endpoint enabled ( <i>Default</i> )
1111	Internal CPU is disabled. SPI client (QSPI0) interfaces are enabled and not exposed.

When strapped to '0001', the LAN9662 embedded CPU is enabled and uses its QSPI0 boot controller interface, which is connected to an optional NOR Flash device, as the second stage bootloader in a secure boot environment. This setting, however, requires the Flash device to be (pre-)programmed with a suitable bootloader. The bootloader can be used to give network access to the LAN9662.

The boot mode using TF-A monitor on UART (FLEXCOM 3b) is also found in the Expansion header. It can be used to bootstrap the NIC card and hereby control the programming of the on-board NOR Flash device. Microchip provides a browser-based update utility called `fwu.html` (can be found at <https://github.com/microchip-ung/arm-trusted-firmware/releases>).

## 4.1.2 PLL Strapping

The LAN9662 PLL strapping, `PLL_STRP[1, 0]`, which is located on `GPIO[36, 27]`, is set to have 25 MHz for both the core clock and the SerDes/PHY clock.

**TABLE 4-2: PLL STRAPPING MODES**

Pulls	PLL_STRP[1:0] Description
00	SerDes: 25 MHz, Cu PHY: 25 MHz (default)
01	SerDes: 125 MHz, Cu PHY: 125 MHz
10	SerDes: 125 MHz, Cu PHY: 25 MHz
11	Reserved

The NIC card supports a single 25 MHz clock source from either an XTAL or OSC. The board is currently populated with a 25 MHz XTAL, VXM7-9013 as reference input.

## 4.1.3 SPI NOR Flash Device (Optional)

The EVB-LAN9662-NIC is equipped with a 2 MB NOR QSPI boot Flash device, SST26VF016B (8-pin SOIC), which is intended for setting up the PCIe end-node to other settings than what is provided through the internal ROM code, like the enumeration scheme or behavior of PCIe.nPERST. The NOR Flash device can be removed if PCIe endpoint interface is used in its standard configuration mode.

## 4.1.4 SPI NOR Flash Device Programming

The NOR Flash device can be programmed using an external Flash programmer connected to the QSPI0 pins in the Expansion header, J2.

To connect the Universal Programmer from ASIX (Forte or Presto), see Table 4-3 for the connections.

**TABLE 4-3: PROGRAMMING SIGNALS**

Expansion Header	Description - Universal Programmer from ASIX
Pin 1 (VccSPI)	P3 (VDD) (Red)
Pin 22 (nMR) *	Pin 20 (GND)
Pin 35 (SI.D1)	P7 (DO/I) (White)
Pin 36 (SPI.nCS0) or 37	P1 (P) (Yellow)
Pin 38 (SI.D0)	P5 (DI/D) (White)
Pin 39 (GND)	P4 (GND) (Blue)
Pin 40 (SI.CLK)	P6 (C) (Green)

**Note 1:** The LAN9662 must not drive the SI.CLK and SI.D0 outputs while programming the SPI Flash device. This is done effectively by strapping nMR, pin 22 to the ground, pin 20 in the Expansion header, and setting SW1 to the 'Local Reset' position.

## 4.1.5 PCIe® Endpoint

The LAN9662 implements a single-lane PCIe Gen2 endpoint controller that can be connected to any PCIe-capable system. The PCIe interface can be used by an external CPU to read or write switch registers.

**Note:** The LAN9662 has frame-DMA capabilities. Frame injection and extraction rates depend on the frame size, as the major overhead sets up the DMA. However, a powerful external CPU system should reach the 1G line rate.

The PCIe edge signal nPERST is used to reset the LAN9662 PCIe endpoint controller. An on-board slide switch, SW1, can select to use the PCIe reset signal to make a complete NIC card reset instead. For maximum interoperability, it is recommended that the SW1 is set to perform this card reset when PCIe nPERST is asserted. SW1 should be in the "PCIe Reset" position.

The PCIe standard requires that the PCIe link is ready in less than 20 ms after PCIe.nPERST is released. This is enough time for configuring the PCIe endpoint controller.

The LAN9662 TX direction has AC coupling. A similar setup is expected for the PCIe host. Likewise, the received REFCLK (PCIe.CLK) is expected to be AC-coupled, and it is thus locally biased to VPTX\_P/2.

Both PCIe.nPERST and PCIe.nWAKE are locally pulled to 3V3AUX from the Edge connector. PCIe.nCLKREQ is pulled to GND, and PCIe.nPRSNT1 is interconnected with PCIe.nPRSNT2.

## 4.1.6 Optional—System Management Bus

SMBus connection can optionally be supported through the PCIe Edge connector, when properly supported in software controlling the FLEXCOM 4b, I<sup>2</sup>C interface.

The NIC card can provide manufacturer information, indicate its model or part number, save its state for a suspend event, report different types of errors, accept control parameters and/or return status.

**Note:** The FLEXCOM 4b, I<sup>2</sup>C interface is shared with the Expansion header, so R63 and R64 must be mounted to connect it to the SMBus.

SMBus is currently not supported by the SW (or internal ROM code).

Through a resistor strap and pin header mount option, the NIC card can optionally provide a standard 10-pin (0.05") ARM CPU DEBUG header, J3, to be used for ICE. The ICE can be used for debugging functions, such as downloading code and single-stepping through programs if the internal CPU is enabled.

[illegible]

The CPU TAP controller mode is set through **JTAG[1:0]** located on GPIO38 and GPIO37, respectively. These pin strappings are currently set for '01', CPU debug.

To connect an ICE to the DEBUG interface, refer to [Table 4-4](#).

Pin	JTAG	In/Out	Description
1	3.3V	—	Power
2	TMS	VIS (PU)	Test mode select input
3	GND	—	Ground
4	TCK	VIS (PU)	Test clock input
5	GND	—	Ground
6	TDO	VO (PU)	Test data output
7	—	—	NC
8	TDI	VIS (PU)	Test data input

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**TABLE 4-4: JTAG HEADER PIN DESCRIPTION (CONTINUED)**

Pin	JTAG	In/Out	Description
9	nDETECT	VIS (PU)	Voltage sense
10	nCARDRST	VIS (PU)	HW reset

**Note 1:** The JTAG signals are not 5V-tolerant. JTAG signal levels are determined by the **VDD\_IOB** power supply pin, which is set to 3.3V on EVB-LAN9662-NIC. **VDD\_IOB** can also be set to 1.8V or 2.5V.

## 4.2 ETHERNET PORTS

The LAN9662 has four logical Ethernet ports exposed to various interfaces. The EVB-LAN9662-NIC uses two internal Cu PHYs (ports 0 and 1) and two SerDes interfaces (ports 2 and 3).

The SerDes interfaces are used with SFP connections. The SerDes signals are not AC-coupled to ensure Common-mode voltage compatibility, as this is mandatory for an SFP module.

### 4.2.1 PHY MII-Management

The LAN9662 serves the internal Cu PHYs over an internal MII-Management bus 1 interface.

### 4.2.2 PHY Copper Interface

The LAN9662 built-in Cu PHYs integrate all passive components required to connect the PHYs' line-side interface to an external 1:1 transformer and Common-mode choke. This reduces the number of components in a design and significantly simplifies the layout of this interface.

The PHYs support auto-negotiation and downshift, and can automatically detect the speed of a link if auto-negotiation is disabled, and thus provides the appropriate connection (called parallel detect).

The PHYs include Automatic Crossover Detection functionality for all speeds (HP Auto MDI/MDI- X™ function) and the ability to detect and correct polarity errors on all MDI pairs. These functions are normally enabled but can be disabled.

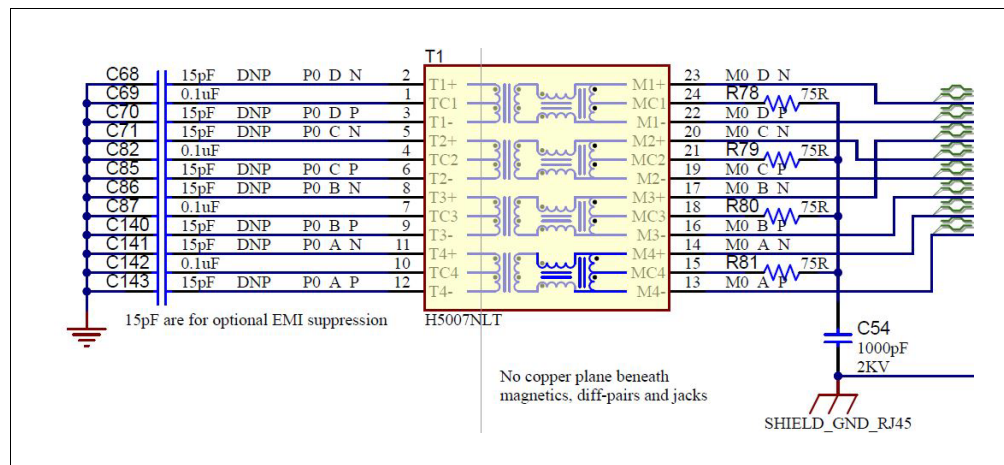
The PHYs support the IEEE standard range of 1m to 100m using twisted pair cabling, however:

- 1000BASE-T mode requires Category 5 enhanced cable in accordance to the cabling specifications defined by IEEE802.3-2005.
- 100BASE-TX mode requires Category 5 cable and 10BASE-T requires Category 3 cable as specified in ISO/IEC 11801.

### 4.2.3 Discrete Magnetic and RJ45 Connector

The EVB-LAN9662-NIC uses two discrete 12-core magnetic modules, H5007NLT from Pulse Electronics intended for Voltage mode PHYs and a 1x2 RJ45 connector, SS-7488S-YG-PG4-BA with integrated green and yellow LEDs.

**FIGURE 4-3: 12-CORE DISCRETE MAGNETIC**



**Note:** Using quality magnetics has significant influence on the EMI performance.

## 4.2.4 SFP Connectors

To support the SFP MSA-defined signals, various LAN9662 GPIO pins are used. [Table 4-5](#) shows the different SFP signals mapping to LAN9662 GPIO pins, some of which have specific functionality.

**TABLE 4-5: SFP SIGNAL MAPPING TO GPIO PINS**

GPIO	ALT mode	In/Out	Description
0	0	Out	SFP0.TXDIS, Tx Disable
1	0	Out	SFP1.TXDIS, Tx Disable
2	0	In (PU)	SFP0.TXFAULT, Tx Fault
3	0	In (PU)	SFP1.TXFAULT, Tx Fault
4	0	Out	SFP0.RS0, Rate Select 0
5	0	Out	SFP0.RS1, Rate Select 1
6	0	Out	SFP1.RS0, Rate Select 0
7	0	Out	SFP1.RS1, Rate Select 1
9	1	Out	Unused - FLEXCOM 0a – SCL
10	1	In/Out (PU)	SFP.SDA, I2C data, FLEXCOM 0a – SDA
18	5	In (PU)	SFP0.MODEDET, Module Detect, IRQ_IN2_C
19	5	In (PU)	SFP1.MODEDET, Module Detect, IRQ_IN3_C
25	6	In (PU)	SFP0.LOS, Rx Loss of Signal, SFP_SD1 – external signal detect input
26	6	In (PU)	SFP1.LOS, Rx Loss of Signal, SFP_SD2 – external signal detect input
76	5	Out (PU)	SFP0.SCL, I2C clock, TWI_SCL_GATE15
77	5	Out (PU)	SFP1.SCL, I2C clock, TWI_SCL_GATE16

**Note 1:** PU = Pull-up to 3.3V

The LAN9662 FLEXCOM 0a drives the I<sup>2</sup>C SCL and SDA signals to the two SFP slots, so that the SFP modules can be auto-detected.



## 4.2.5 Serial-GPIO for Port Status LED Control

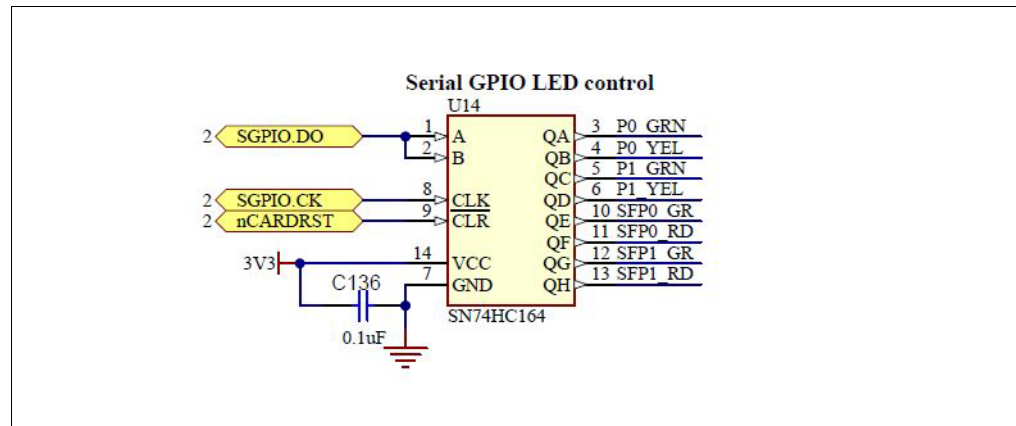
Port status LEDs are automatically controlled by LAN9662 using its serial GPIO interface. The serial-GPIO engine is configured to have two bits per SGPIO port. In this mode, internal devices 0-3 maps to SGPIO ports 0-3.

- Output SGPIO ports 0: Cu port P0 – control LEDs in RJ45 connector J4, green and yellow
- Output SGPIO ports 1: Cu port P1 – control LEDs in RJ45 connector J6, green and yellow
- Output SGPIO ports 2: SFP port S0 – control bi-color LED D2, green and red
- Output SGPIO ports 3: SFP port S1 – control bi-color LED D3, green and red

Copper ports use a green LED to indicate 1G link and yellow for 10/100M. The SerDes ports use a green LED for 1G/2.5G link and red LED for 100M. Solid light indicates link-up and blinking means traffic through the port.

Figure 4-4 shows how the conversion from a serial bit stream is made using an 8-Bit Parallel-Out Serial Shift Register, SN74HC164. The serial GPIO 'Load' signal, which is intended to hold the current state in the register, is not used as the human eye cannot detect the fast changes when the serial bit stream is clocked through the shift registers.

**FIGURE 4-4: SERIAL-GPIO – PORT STATUS LED CONTROL**



## 4.3 SMA CONNECTORS

The EVB-LAN9662-NIC provides two SMA connectors for PTP applications. One is used as 1PPS output, J9, and the other as 1PPS input, J7.

The SMA input is connected to LAN9662 PTPSYNC4 engine using GPIO39. The input is LVTTTL and 3V3-tolerant. It is not 5V-tolerant. The SMA output is connected to LAN9662 PTPSYNC3 engine using GPIO38. The output uses LVTTTL levels.

Both SMA connectors are circuit-protected using BAS70-04 voltage clamping diodes.

## 4.4 ePPS HEADER

A 10-pin, 0.1" right-angle header (J8) is provided for internal ePPS/PPS distribution. The ePPS header exposes three LAN9662 PTPSYNC (0-2) signals.

Table 4-6 describes the location within the ePPS header.

**TABLE 4-6: ePPS HEADER DESCRIPTION**

Pin	Signal	ALT Mode	In/Out	Description
1	GND	—	—	Ground
2	GPIO35	2	Out	ePPS/PPS0 In/Out
3	GND	—	—	Ground
4	GPIO36	2	Out	ePPS/PPS1 In/Out
5	GND	—	—	Ground
6	GPIO37	2	Out	ePPS/PPS2 In/Out
7	GND	—	—	Ground
8	—	—	—	NC
9	—	—	—	NC
10	GND	—	—	Ground

## 4.5 RTE HEADER

A 10-pin, 0.1" header (J10) is used to expose the LAN9662 RTE features by providing the RTE-associated SPI control interface, QSPI1, to the RTE client. Two input/output (I/O) configurable (RTE) triggers are also provided.

Table 4-7 describes the location of these signals within the RTE header.

**TABLE 4-7: RTE HEADER DESCRIPTION**

Pin	Signal	ALT Mode	In/Out	Description
1	3.3V	—	—	Power
2	GPIO16	4	Out	IOB_TRG0, OB_TRG_0
3	GPIO17	2	In	IOB_TRG1, IB_TRG_1
4	GPIO59	1	Out	QSPI1.SCK
5	GPIO61	1	In/Out	QSPI1.D0
6	GPIO62	1	In/Out	QSPI1.D1
7	GPIO63	1	In/Out	QSPI1.D2
8	GPIO64	1	In/Out	QSPI1.D3
9	GPIO60	1	Out	QSPI1.nCS
10	GND	—	—	Ground



**TABLE 4-8: EXPANSION HEADER PIN DESCRIPTION**

Pin	Signal	Description	Pin	Signal	Description
1	3V3	3.3V power from PCIe Edge	2	5V	NC (See Note 1)
3	GPIO 48	I <sup>2</sup> C SDA (FC1c)	4	5V	NC (See Note 1)
5	GPIO 47	I <sup>2</sup> C SCL (FC1c)	6	GND	—
7	GPIO 39	(PTP4_IN)	8	GPIO 53	UART TX (FC3b)
9	GND	—	10	GPIO 52	UART RX (FC3b)
11	GPIO 49	CE (FCS7)	12	GPIO 42	CE (FCS3)
13	GPIO 54	(IRQ3 or TRG3_C)	14	GND	—
15	GPIO 30	(CAN1_Rx)	16	GPIO 31	(CAN1_Tx)
17	3V3	3.3V power from PCIe Edge	18	GPIO 37	(PTP2_OUT)
19	GPIO 45	MOSI (FC2b)	20	GND	—
21	GPIO 44	MISO (FC2b)	22	GPIO 56	(nMR)
23	GPIO 43	SCLK (FC2b)	24	GPIO 40	CE (FCS1)
25	GND	—	26	GPIO 41	CE (FCS2)
27	GPIO 58	I <sup>2</sup> C SDA (FC4b)	28	GPIO 57	I <sup>2</sup> C SCL (FC4b)
29	GPIO 35	(CAN0b Rx/PTP0 IN)	30	GND	—
31	GPIO 36	(CAN0b Tx/PTP1 OUT)	32	GPIO 51	(PWM_B)
33	GPIO 65	—	34	GND	—
35	QSPI.D1	SPI.D1	36	QSPI.nCS0	SPI.nCS0 (LAN9662)
37	GPIO 50	(SPI.nCS_NOR)	38	QSPI.D0	SPI.D0
39	GND	—	40	QSPI.CLK	SPI.CLK

**Note 1:** FC = Flexcom, FCS = Flexcom Shared; NC = Not connected. The header does not provide the normal 5V, only 3.3V.

# EVb-LAN9662-NIC Hardware Details

## 4.7 GPIO USAGE OVERVIEW

The LAN9662 GPIOs can be configured for multiple different interfaces and only a small subset is used on the NIC card. [Table 4-9](#) shows which GPIOs and functionality have been used. Strapping pins are marked in orange.

**Note:** Usage that results in changes to the Raspberry Pi HAT signals compared to EV18W53A (UNG8290) and EV09D37A (UNG8291) are marked in green.

**TABLE 4-9: GPIO USAGE**

GPIO	Alt Mode	Connected To	GPIO	Alt Mode	Connected To
0	0	SFP0.TXDIS, Tx Disable	40	1	HAT, CE (FCS1)
1	0	SFP1.TXDIS, Tx Disable	41	1	HAT, CE (FCS2)
2	0	SFP0.TXFAULT	42	1	HAT, CE (FCS3)
3	0	SFP1.TXFAULT	43	1	HAT, SPI.SCLK (FC2b)
4	0	SFP0.RS0, Rate Select bit 0	44	1	HAT, SPI.MISO (FC2b)
5	0	SFP0.RS1, Rate Select bit 1	45	1	HAT, SPI.MOSI (FC2b)
6	0	SFP1.RS0, Rate Select bit 0	46	—	NC
7	0	SFP1.RS1, Rate Select bit 1	47	1	HAT, I <sup>2</sup> C CLK (FC1c)
8	—	NC	48	1	HAT, I <sup>2</sup> C SDA (FC1c)
9	1	NC (I <sup>2</sup> C SCL, FC0a)	49	1	HAT, CE (FCS7)
10	1	SFP.SDA (I2C SDA, FC0a)	50	0	HAT
11	—	NC	51	(5)	HAT, (PWM_B)
12	—	NC	52	1	HAT, UART RX (FC3b)
13	—	NC	53	1	HAT, UART TX (FC3b)
14	—	NC	54	(2-6)	HAT, (IRQ/TRG)
15	—	NC	55	—	NC
16	2	RTE, IOB_TRG0 (IB_TRG_0)	56	0	HAT, (nMR), Master Reset
17	4	RTE, IOB_TRG1 (OB_TRG_1)	57	1	HAT, SCL (FC4b), EEPROM
18	2	SFP0.MODEDET (IRQ_IN2)	58	1	HAT, SDA (FC4b), EEPROM
19	2	SFP1.MODEDET (IRQ_IN3)	59	1	RTE, QSPI1 SCK
20	—	NC	60	1	RTE, QSPI1 nCS
21	—	NC	61	1	RTE, QSPI1 D0
22	—	NC	62	1	RTE, QSPI1 D1
23	—	NC	63	1	RTE, QSPI1 D2
24	—	NC	64	1	RTE, QSPI1 D3
25	6	SFP0.LOS, SD1	65	0	HAT
26	6	SFP1.LOS, SD2	66	—	NC
27	0	PLL_STRP0	67	—	NC
28	2	PCIe.WAKE#	68	—	NC
29	2	PCIe.PERST#	69	—	NC
30	(2)	HAT (CAN1_Rx)	70	—	NC

**Note 1:** FC = Flexcom, FCS = Flexcom Shared; NC = Not connected

**TABLE 4-9: GPIO USAGE (CONTINUED)**

GPIO	Alt Mode	Connected To	GPIO	Alt Mode	Connected To
31	(2)	HAT (CAN1_Tx)	71	—	NC
32	3	SGPIO.CK, LED	72	—	NC
33	3	SGPIO.DO, LED	73	—	NC
34	—	—	74	—	NC
35	2	HAT, ePPS, PTP0_OUT	75	—	NC
36	2	HAT, ePPS, PTP1_OUT	76	5	SFP0.SCL, TWI_SCL_GATE15 (FC0a)
37	2	HAT, ePPS, PTP2_OUT	77	5	SFP1.SCL, TWI_SCL_GATE16 (FC0a)
38	2	SMA 1PPS out, PTP3_OUT	—	—	—
39	2	SMA 1PPS in, HAT (PTP4_IN)	—	—	—

**Note 1:** FC = Flexcom, FCS = Flexcom Shared; NC = Not connected

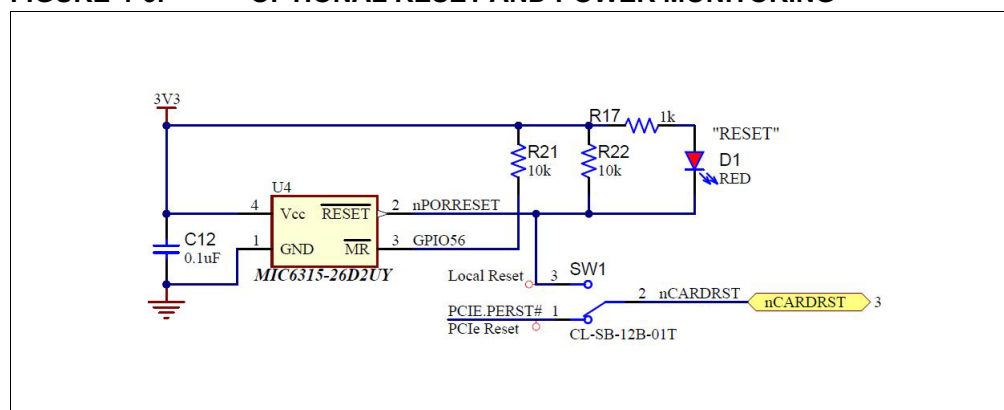
## 4.8 OPTIONAL RESET AND POWER MONITORING

The PCIe host/Edge connector normally controls the whole NIC card hardware reset through its PWRGD signal that is connected to the local PCIe.PERST# (that is, when the slide switch, SW1, is in the 'PCIe Reset' position).

It is however possible to change this reset scheme to a more local POR approach to control the NIC card hardware reset, when the slide switch is in 'Local Reset' position. This mode is intended for standalone use, where the NIC card operates more locally and is managed by the LAN9662 internal CPU. Thus, hardware reset can also be initiated from the LAN9662 itself through GPIO56. In this position, the PCIe host can still use the local PCIe.PERST#, but it will only reset the PCIe end-node controller when LAN9662 is set up to support it.

In the 'Local Reset' position, a voltage supervisor, MIC6315-26D2UY, is used to hold the NIC card in POR state until the 3.3V board supply is up. MIC6315 provides a manual reset (nMR) input, which is connected to the LAN9662 GPIO56. A red LED (D1) is controlled by the POR output signal and is used to indicate the Reset state.

**FIGURE 4-6: OPTIONAL RESET AND POWER MONITORING**





**NOTES:**



## Appendix A. PCB Layout and Silk Screens

### A.1 INTRODUCTION

#### A.1.1 Outline

The EVB-LAN9662-NIC reference design uses a standard PCIe card form factor with the RJ45, SFP and SMA (for 1PPS in/out) connectors in the bracket. The board length is determined by the PCIe x1 connector length and the height is determined by the PC bracket size. The EVB-LAN9662-NIC dimensions are 111.20x83.65x1.60 mm. [Figure A-1](#) shows the outline of EVB-LAN9662-NIC.

**FIGURE A-1: EVB-LAN9662-NIC OUTLINE**



The LAN9662 package pinout is specifically optimized for low-cost PCB designs. As a result, the EVB-LAN9662-NIC has only four PCB layers.

## EVB-LAN9662-NIC User's Guide

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All signals are routed on the top and bottom layers, 1 and 4. Layer 2 is a solid ground plane, which is also used to remove heat from components, and it must (also for this reason) be ensured that good connection between the outer layer ground fills and the ground planes are established.

[Table A-1](#) lists the different layers in the EVB-LAN9662-NIC.

**TABLE A-1: EVB-LAN9662-NIC PCB LAYERS AND DESCRIPTIONS**

Layer	Description
1 (TOP)	LAN9662 signal traces and SerDes paths
2 (GND)	Solid ground plane
3 (POWER)	Power planes for LAN9662: 1.1V and 3.3V
6 (BOTTOM)	LAN9662 signal traces

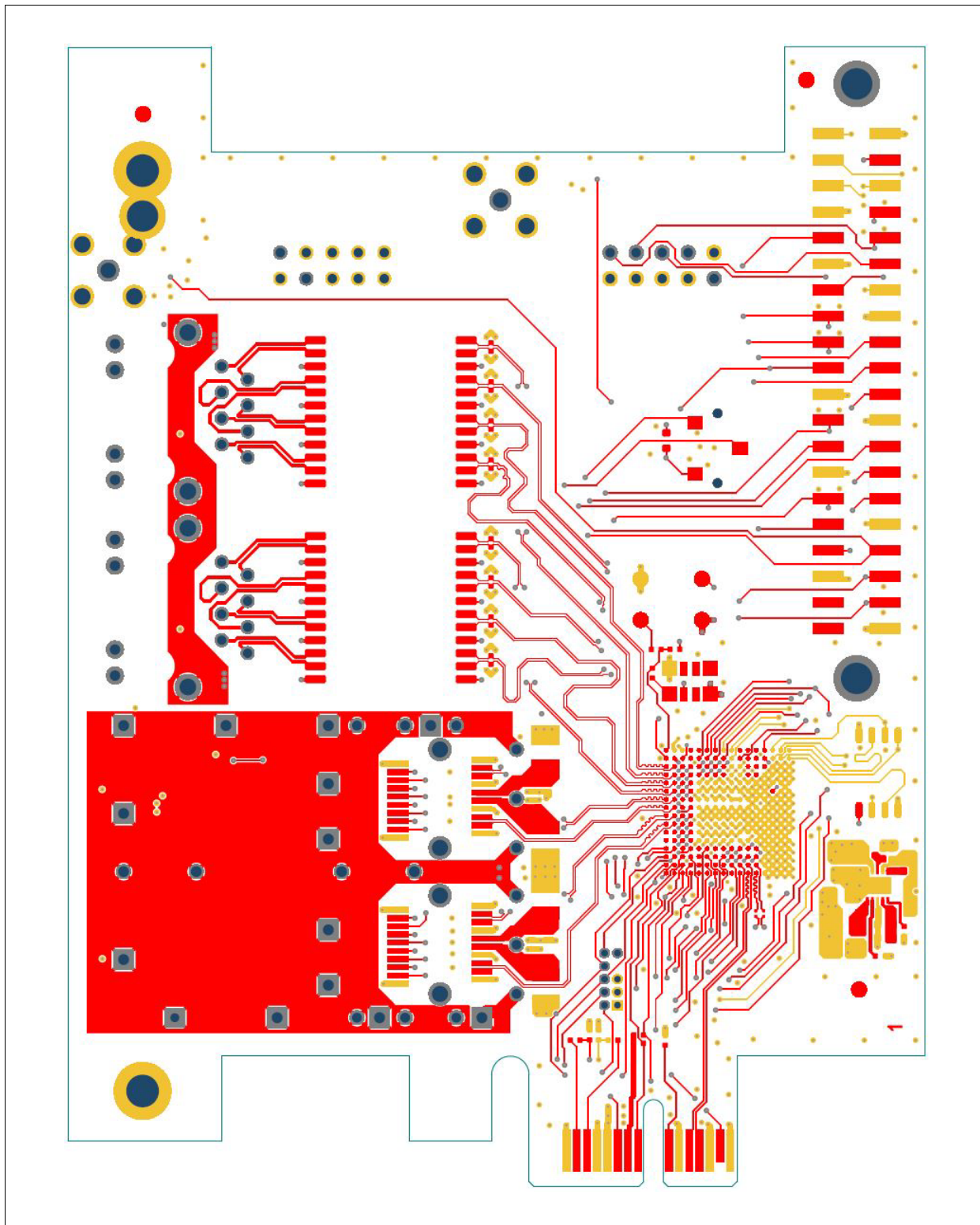
The ground shield found on the top and bottom layer serves as a “quiet” ground. It is connected via an RC network to the ground plane, providing a low-impedance return path for high-frequency noise.



### A.1.3 Layer 1 (TOP)

The larger areas in red in [Figure A-3](#) indicates the shield ground areas.

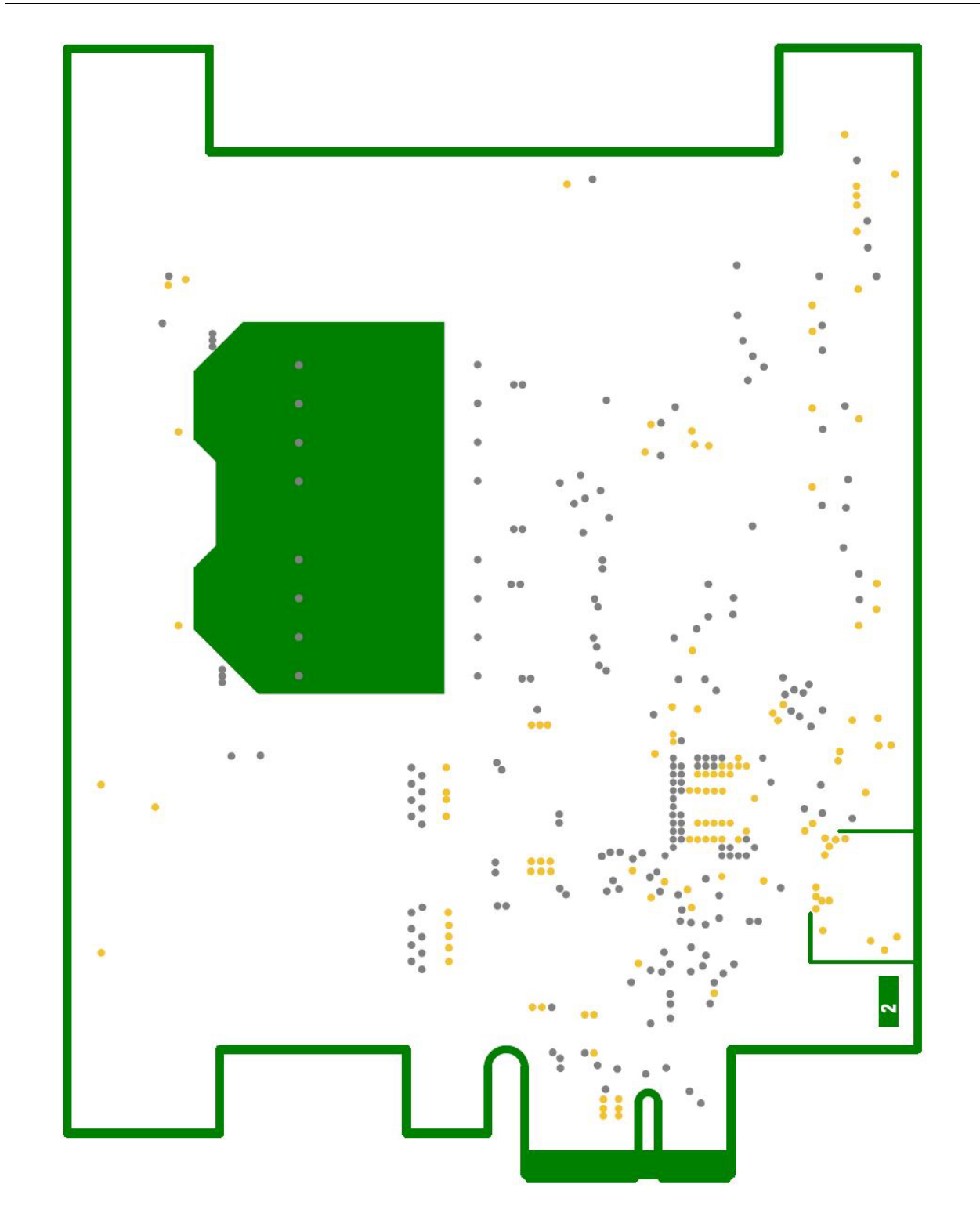
**FIGURE A-3: EVB-LAN9662-NIC LAYER 1**



## A.1.4 Layer 2 (GND)

The larger areas in green in [Figure A-4](#) indicates an area without copper.

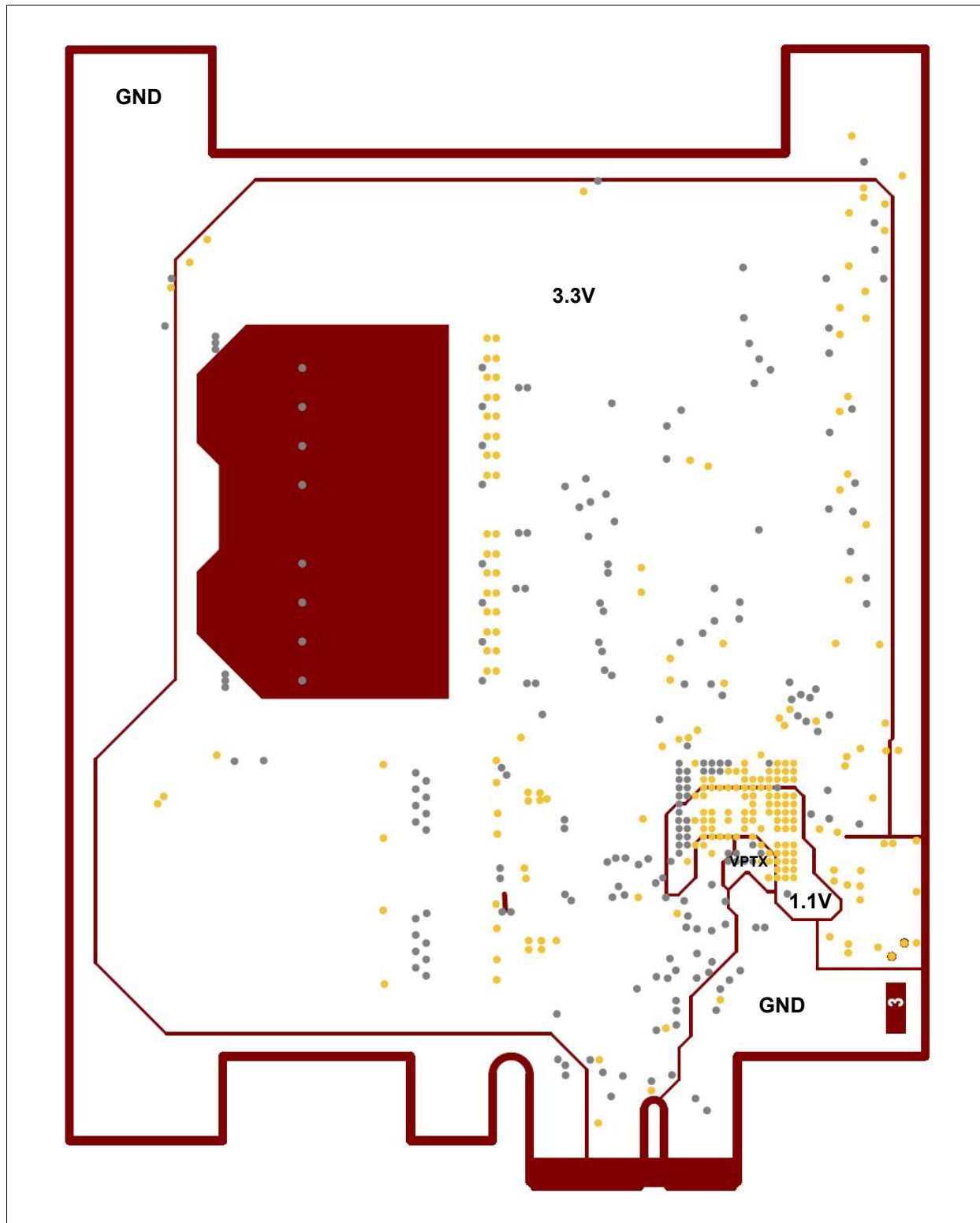
**FIGURE A-4: EVB-LAN9662-NIC LAYER 2**



### A.1.5 Layer 3 (POWER and GND)

The larger areas in red in [Figure A-5](#) indicates an area without copper.

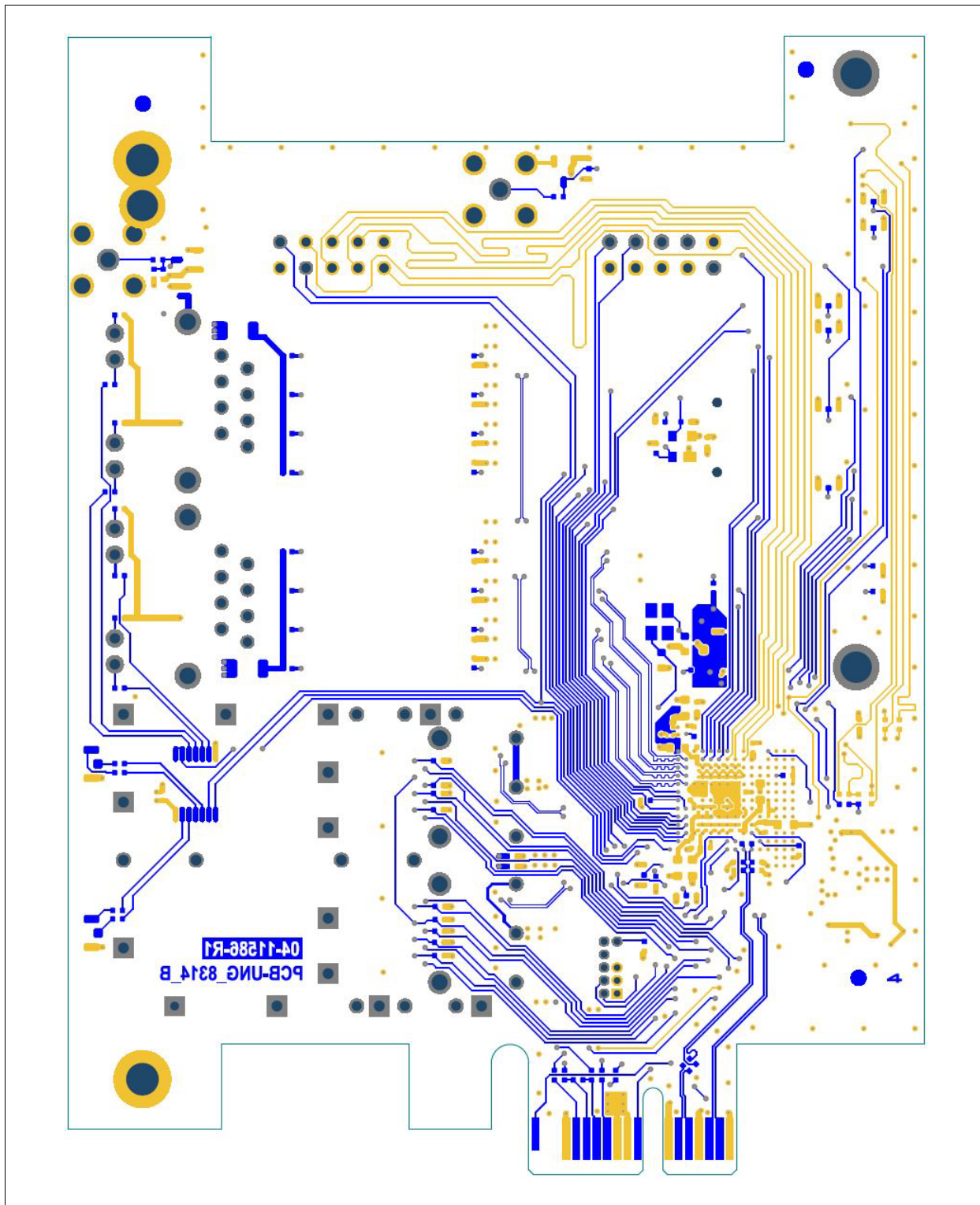
**FIGURE A-5: EVB-LAN9662-NIC LAYER 3**





## A.1.6 Layer 4 (BOTTOM)

FIGURE A-6: EVB-LAN9662-NIC LAYER 4







# PCB Layout and Silk Screens

## A.1.8 PCB Layer Stack-up

The EVB-LAN9662-NIC is a 4-layer impedance-controlled PCB. [Figure A-8](#) shows the stack-up.

**FIGURE A-8: EVB-LAN9662-NIC PCB STACK-UP**

Board Stack Report					
Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	LPI-Green	0,50mil	3,5
4		Top Layer 1	Copper	2,01mil	
5		Dielectric1	PP-370HR-1x106_1080_58	4,29mil	4,04
6		Inner Layer 2	Copper	1,38mil	
7		Dielectric 2	CR-370HR-47mil	47,00mil	4,4
8		Inner Layer 3	Copper	1,38mil	
9		Dielectric 3	PP-370HR-1x106_1080_58	4,29mil	4,04
10		Bottom Layer 4	Copper	2,01mil	
11		Bottom Solder	LPI-Green	0,50mil	3,5
12		Bottom Overlay			
13		Bottom Paste			
Height : 63,36mil					

## A.2 PCB TRACE WIDTHS AND CLEARANCE

- EVB-LAN9662-NIC board thickness: 1.6 mm  $\pm$ 10%
- Characteristic impedance single-ended: 50 $\Omega$  or 60 $\Omega$
- Characteristic impedance differential signals: 100 $\Omega$
- Single-ended trace width: 125  $\mu$ m and 150  $\mu$ m
- Single-ended trace-to-trace clearance: 400  $\mu$ m
- 100 ohm differential trace width: 125  $\mu$ m
- 100 ohm differential trace-to-trace spacing: 220  $\mu$ m

**TABLE A-2: NET IMPEDANCE AND LENGTH MATCHING**

Net Group Name	Type	Impedance	Length Matching	Tolerance (mm)	Max Vias	Via type	Layers	Notes
Clock	Single-ended	50 $\Omega$	None	—	4	All	All	—
SI	Single-ended	50 $\Omega$	None	—	4	All	All	Daisy-chain
DiffClock	Differential	100 $\Omega$	P/N only	1	2	All	All	—
SerDes	Differential	100 $\Omega$	P/N only	0	2	—	Outer	See Note 1
Sense	Analog	—	—	—	—	All	All	—
Power	Power	—	—	—	—	—	—	—
Static	Single-ended	—	—	—	—	—	All	See Note 2
Unspecified	Single-ended	60 $\Omega$	—	—	—	—	All	See Note 3

- Note 1:** Differential signal on outer layers.
- 2:** No impedance => 4mil trace on any layer.
- 3:** Any unspecified nets should be routed as 60 $\Omega$ .

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**NOTES:**

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