

# IRS2975C Data Sheet

## Infineon® REAL3™ 3D Image Sensor

### Features

- ToF-Pixel-Array
  - Array of 43200 ToF-pixels (240 columns, 180 rows)
  - Pixel size 10 x 10  $\mu\text{m}$ , array size 2.40 x 1.80 mm (image circle 3 mm)
  - 10  $\mu\text{m}$   $\mu\text{Lens}$  pitch
  - Each ToF-pixel is measuring distance and brightness
  - Each ToF-pixel equipped with a patented circuitry for suppression of background illumination (SBI) enabling extended dynamic range at bright ambient light as well as for active illumination.
  - Voltage controlled pixel modulation enabling high modulation bandwidth (up to 200 MHz) at low power consumption
- Illumination controller for active light source (VCSEL)
  - 2xLVDS illumination signal output for enhanced signal quality, improved EMC performance and dual driver support
  - Support of module level laser safety: Average and peak current sensing to monitor the power through the illumination source
  - Thresholds and limits for the laser safety supporting functions are loaded during the boot-load process from the module's SPI flash or EEPROM memory
  - Monitor diode support for broken VCSEL diffuser or close object detection
  - 3rd party VCSEL driver support (3 wire interface, APC\_Gate and error handling)
  - Fine adjustment of optical output power to compensate VCSEL production spread
- Modulation controller for ToF-pixel array and illumination
  - Widely configurable distance precision through adjustable modulation bandwidth
  - Enhanced modulation coding to limit the ambiguity range and reduced calibration effort
  - Modulation frequency spreading to enable multi-camera support and improve EMC performance
  - Phase and delay configuration to support distance dependent error calibration
  - On-chip pixel-array temperature sensor and support of external low cost NTC sensor for measurement of illumination temperature for thermal depth correction
- Programmable sequence controller for autonomous frame streaming
  - Programmable sequence scheduler with up to 64 measurements per depth frame
  - Flexible illumination schemes to allow for high frame rates and fast object tracking
  - Mixed mode for simultaneous execution of multiple use case (e.g. 5 fps long-range-mode for room awareness interleaved with 50 fps short-range-mode for finger tracking)
- Digital high-speed readout
  - On-chip high-speed analogue to digital conversion - full digital readout with 12 bit resolution
  - Ultra-short readout time: <880  $\mu\text{s}$  for full-resolution phase frames
  - MIPI compliant CSI-2 interface: 2-data lanes each 1 Gbit/s
  - MIPI compliant CCI (Camera Control Interface) for image sensor configuration
- Low power design for mobile devices with reduced idle current consumption
- On-chip core supply generated from 1V8 I/O supply domain
- Drop-in replacement for IRS2875C with enhanced pixel performance
- Support of SPI flash or I2C EEPROM memory for calibration data and self-booting options
- Unique chip ID for digital image sensor identification
- Bare-die image sensor (4.6 x 4.1 mm) for chip-on-board mounting: highest flexibility in camera module design and smallest module size

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**Potential applications**

A detailed listing of the parameters is summarized in Chapter 5.

## Potential applications

Due to the optimized design of the IRS2975C a lot of different applications are possible. Nevertheless, the main target application for the 3D image sensor is mobile devices.

### Applications

- Mobile devices (e.g. smart phones, AR/VR headsets)
  - Secure face recognition and face motion tracking
  - SLAM - simultaneous localization and mapping
  - 6-degree-of-freedom (6-DoF) inside-out self-localization based on distance measurement to room boundaries
  - 3D reconstruction (room, object and body scanning)
  - Virtual- & augmented reality (AR/VR)
  - High quality photo camera support (autofocus, computational photography)
  - Hand and finger tracking for gesture control and interaction with virtual objects
- Robotics
  - Intelligent guard fencing for enhanced safety of industrial robots
  - SLAM and obstacle detection for advanced navigation
  - Visual support for robot grippers
- Smart home cameras and security cameras
  - Location, tracking and identification of individuals (humans, animals)
  - People counting and motion analysis

## Product validation

Technology qualified for consumer applications.

Ready for validation in applications listed above based on the test conditions in the relevant tests of IEC 60747 and 60749, or alternatively JEDEC20/22.

## Description

IRS2975C is a 3D Time-of-Flight (ToF) image sensor designed for mobile consumer applications. The high integration level of this single-chip design enables an optimized bill of material, smallest form factors and reduced design complexity. The unique pixel design in a dedicated ToF CMOS process provides outstanding sensitivity and robust indoor and outdoor operation. The high degree of functionality offers highest flexibility to optimize the 3D camera design for different application requirements. Furthermore, IRS2975C can be dynamically configured during operation to optimize the overall camera performance, for example to change operation modes, or update exposure times and to handle more demanding requirements like adapting the frame rate to reduce the power consumption.

IRS2975C is highly optimized for mobile devices by providing a HQVGA pixel resolution (~43k pixel), optimized interfacing and a best depth performance/power consumption ratio.

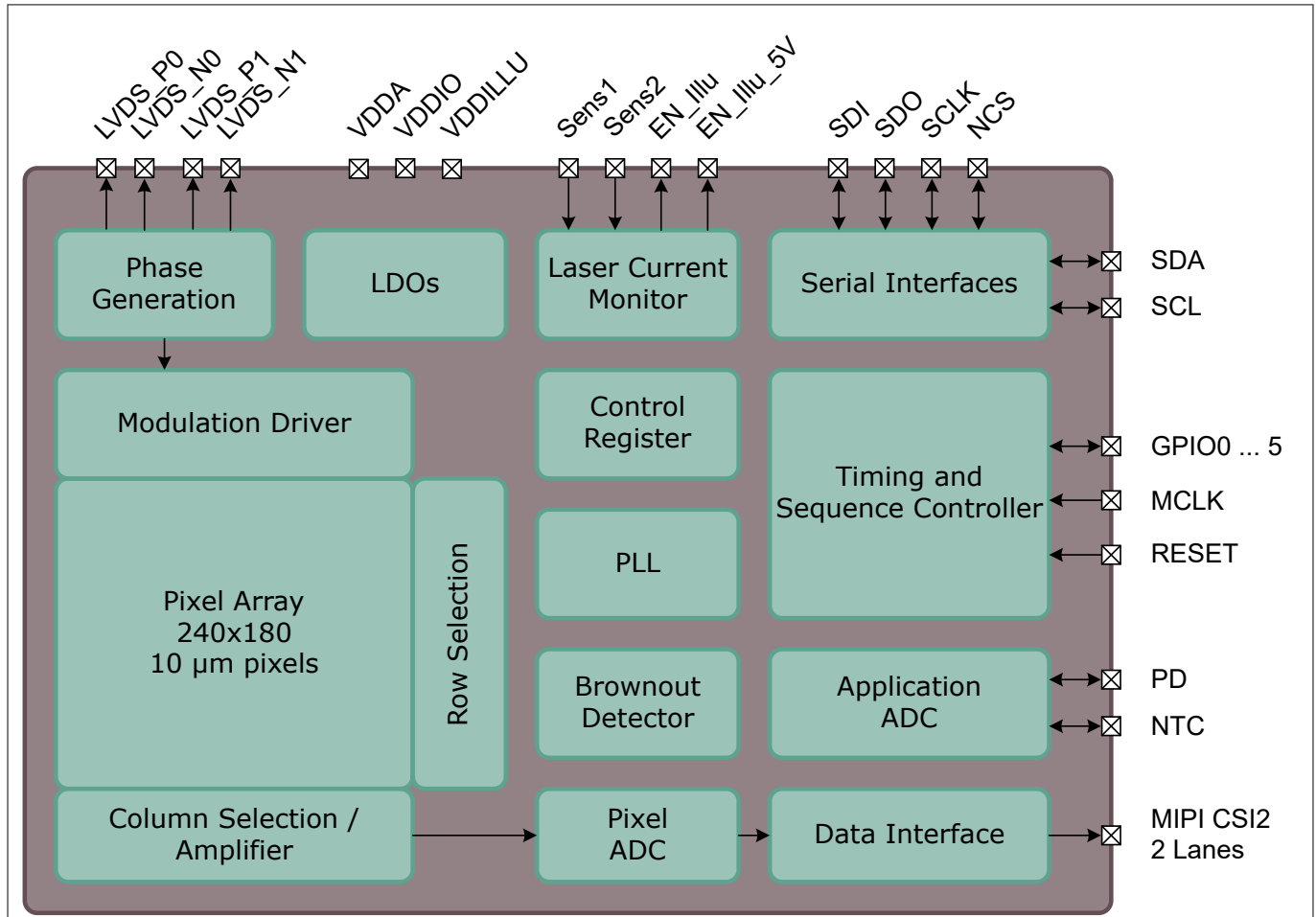
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## 1 Block diagram IRS2975C

### 1 Block diagram IRS2975C

The sensor contains a pixel array with a size of 240 x 180 (~43k) pixels. Within this array the ROI of the device can be adjusted.



**Figure 1** Block diagram

IRS2975C is a SoC integrating all key-functional-blocks required for generating a depth image (Z-image). The internal architecture of the SoC is based on a proprietary bus. The complete signal chain from the PLL to the analog-to-digital conversion is integrated on-chip. The sensor provides fully digitized phase information to the host system using a standardized high speed serial data interface (MIPI CSI-2).

Further auxiliary blocks cover the interface to a SPI Flash, an external temperature sensor and support illumination monitoring functions with a photo diode, or similar.

#### 1.1 System block diagram

There are two major system block and supply concepts:

- Combining the image sensor and the illumination into one module (RX/TX module)
- Separating the image sensor and the illumination into dedicated modules (RX module and TX module)

The IRS2975C supports both topologies while the supply considerations need to be addressed at the schematic level. The RX module topology mainly uses a 2.8V analog sensor supply which is typically also used for RGB image sensors. Within the RX/TX module topology the image sensor supply is derived out of the illumination supply using a LDO or Buck converter. To keep the efficiency as high as possible within the combined module approach a supply voltage of 3.3V of the image sensor can be selected.

## 2 Bare Die, Pads, CRA and Assembly

The analog supply of the image sensor has to be either in the range between 2.6 and 3V (nominal value 2.8V) or between 3.1 and 3.6V (nominal value 3.3V). The selected supply range has to be fixed at camera design and the decision has to be implemented in the schematic accordingly.

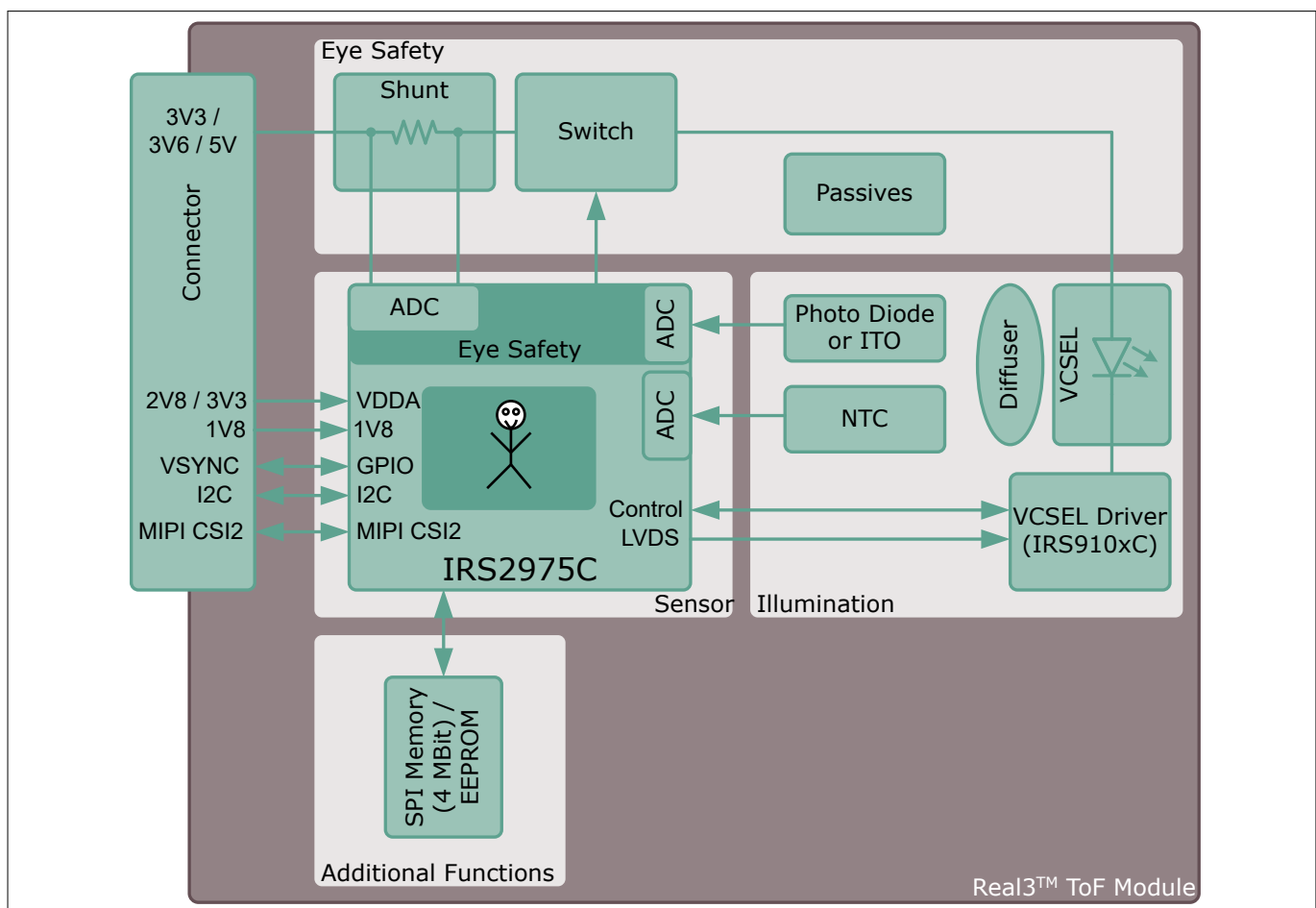
Besides the IRS2975C sensor and the lens, the module contains few external components for laser safety monitoring (only a shunt resistor and a PMOS switch are required). The main monitoring functionality is performed by IRS2975C sensor itself.

The TX part of the system consists of a VCSEL, a laser driver like IRS910xC and a diffuser.

Additional components inside the module are:

- One NTC which is used to monitor the temperature of the VCSEL and
- One SPI flash or I2C EEPROM memory module to store calibration values and operation mode information

Figure 2 shows a block diagram of a typical camera module incorporating IRS2975C



**Figure 2** System block diagram

## 2 Bare Die, Pads, CRA and Assembly

Figure 3 shows the location of the optical area within the IRS2975C.

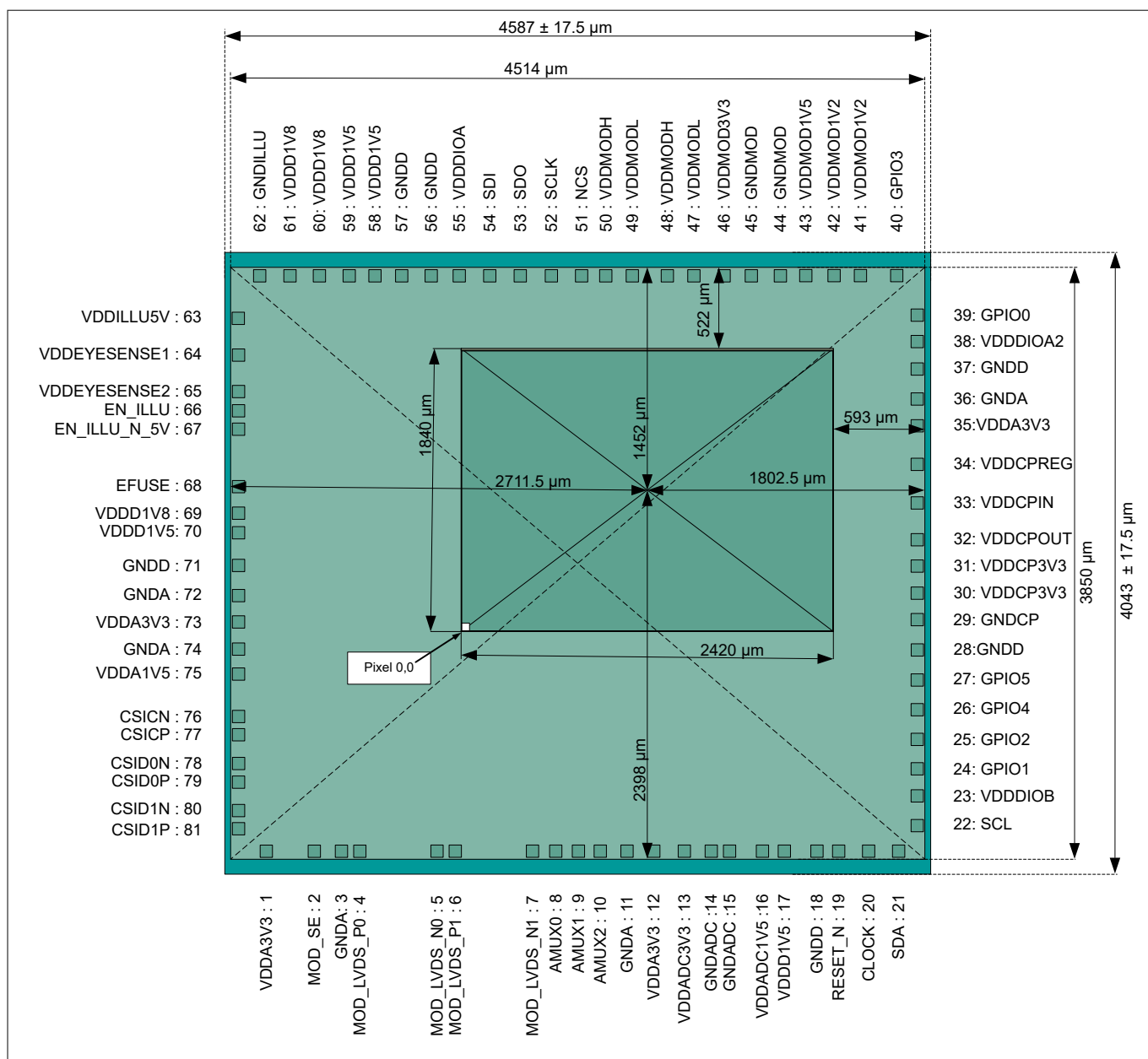
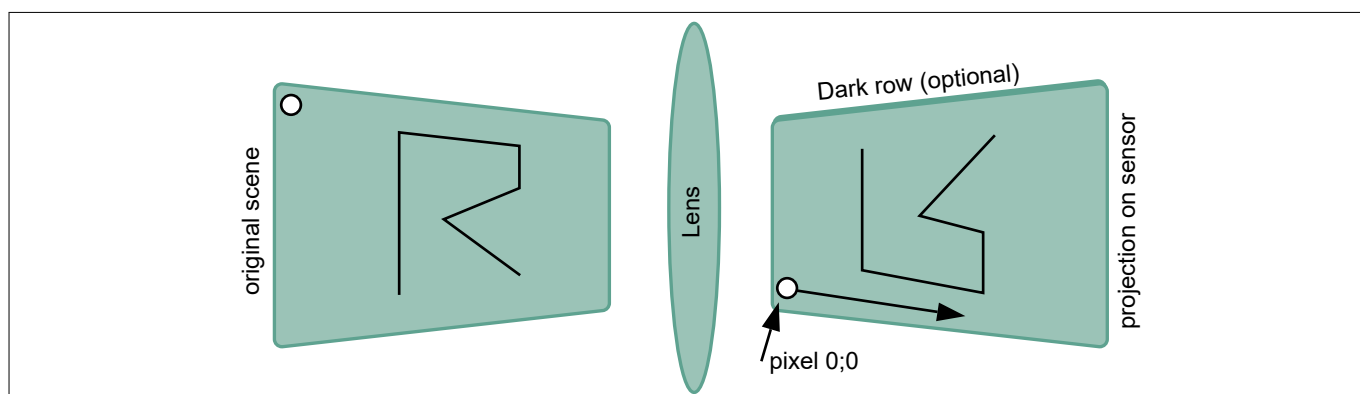
**2 Bare Die, Pads, CRA and Assembly**

**Figure 3 Die Dimensions Overview**

Figure 4 illustrates the pixel readout schema and the orientation of the resulting picture.


**Figure 4 Readout and picture orientation**

**2 Bare Die, Pads, CRA and Assembly**
**2.1 Physical Dimensions**
**Table 1 Physical Dimensions**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Dimension Optical Area x	Size OptX		2400		μm	
Dimension Optical Area y	Size OptY		1800		μm	
Die Size x	Size X	4569.5	4587	4604.5	μm	
Die Size y	Size Y	4025.5	4043	4060.5	μm	
Die Thickness	d	138	150	162	μm	
Bondpad Size x and y		80			μm	
Bondpad Pitch		120			μm	
Pad Construction - Last Material			AlCu			
Pad Construction - Isolation			IMOX			
Passivation			Oxide + SiN			
Chip coating			Without photoimide			
Die backside			Silicon			
Wafer size			8"			

**2.2 Pad Coordinates**

Table 2 defines the pad coordinates of the IRS2975C. The coordinates are based on the light green area of the dimensions within Figure 3.

**Table 2 Pad Coordinates**

Pad no	X [μm]	Y[μm]	dX[μm]	dY[μm]	Pad name
1	227.000	46.000	80.000	80.000	VDDA3V3
2	541.000	46.000	80.000	80.000	MOD_SE
3	716.000	46.000	80.000	80.000	GNDA
4	836.000	46.000	80.000	80.000	MOD_LVDS_P0
5	1338.000	46.000	80.000	80.000	MOD_LVDS_N0
6	1458.000	46.000	80.000	80.000	MOD_LVDS_P1
7	1960.000	46.000	80.000	80.000	MOD_LVDS_N1
8	2114.000	46.000	80.000	80.000	AMUX0
9	2258.000	46.000	80.000	80.000	AMUX1
10	2402.000	46.000	80.000	80.000	AMUX2

(table continues...)

**2 Bare Die, Pads, CRA and Assembly**
**Table 2 (continued) Pad Coordinates**

Pad no	X [μm]	Y [μm]	dX [μm]	dY [μm]	Pad name
11	2577.000	46.000	80.000	80.000	GNDA
12	2752.000	46.000	80.000	80.000	VDDA3V3
13	2950.000	46.000	80.000	80.000	VDDADC3V3
14	3125.000	46.000	80.000	80.000	GNDADC
15	3245.000	46.000	80.000	80.000	GNDADC
16	3457.000	46.000	80.000	80.000	VDDADC1V5
17	3600.000	46.000	80.000	80.000	VDDD1V5
18	3812.000	46.000	80.000	80.000	GNDD
19	3956.000	46.000	80.000	80.000	RESET_N
20	4150.000	46.000	80.000	80.000	CLOCK
21	4344.000	46.000	80.000	80.000	SDA
22	4468.000	223.000	80.000	80.000	SCL
23	4468.000	417.000	80.000	80.000	VDDDI0B
24	4468.000	592.000	80.000	80.000	GPIO<1>
25	4468.000	786.000	80.000	80.000	GPIO<2>
26	4468.000	980.000	80.000	80.000	GPIO<4>
27	4468.000	1174.000	80.000	80.000	GPIO<5>
28	4468.000	1368.000	80.000	80.000	GNDD
29	4468.000	1566.000	80.000	80.000	GNDCP
30	4468.000	1731.000	80.000	80.000	VDDCP3V3
31	4468.000	1906.000	80.000	80.000	VDDCP3V3
32	4468.000	2081.000	80.000	80.000	VDDCPOUT
33	4468.000	2321.000	80.000	80.000	VDDCPIN
34	4468.000	2571.000	80.000	80.000	VDDCPREG
35	4468.000	2824.000	80.000	80.000	VDDA3V3
36	4468.000	2999.000	80.000	80.000	GNDA
37	4468.000	3197.000	80.000	80.000	GNDD
38	4468.000	3372.000	80.000	80.000	VDDDIOA
39	4468.000	3547.000	80.000	80.000	GPIO<0>
40	4331.000	3804.000	80.000	80.000	GPIO<3>
41	4097.000	3804.000	80.000	80.000	VDDMOD1V2
42	3927.000	3804.000	80.000	80.000	VDDMOD1V2
43	3742.000	3804.000	80.000	80.000	VDDMOD1V5

**(table continues...)**



**2 Bare Die, Pads, CRA and Assembly**
**Table 2 (continued) Pad Coordinates**

Pad no	X [μm]	Y [μm]	dX [μm]	dY [μm]	Pad name
44	3572.000	3804.000	80.000	80.000	GNDMOD
45	3387.000	3804.000	80.000	80.000	GNDMOD
46	3207.000	3804.000	80.000	80.000	VDDMOD3V3
47	3012.000	3804.000	80.000	80.000	VDDMODL
48	2837.000	3804.000	80.000	80.000	VDDMODH
49	2608.000	3804.000	80.000	80.000	VDDMODL
50	2438.000	3804.000	80.000	80.000	VDDMODH
51	2281.000	3804.000	80.000	80.000	NCS
52	2081.000	3804.000	80.000	80.000	SCLK
53	1881.000	3804.000	80.000	80.000	SDO
54	1681.000	3804.000	80.000	80.000	SDI
55	1482.000	3804.000	80.000	80.000	VDDDIOA
56	1302.000	3804.000	80.000	80.000	GNDD
57	1107.000	3804.000	80.000	80.000	GNDD
58	937.000	3804.000	80.000	80.000	VDDD1V5
59	767.000	3804.000	80.000	80.000	VDDD1V5
60	572.000	3804.000	80.000	80.000	VDDD1V8
61	381.000	3804.000	80.000	80.000	VDDD1V8
62	183.000	3804.000	80.000	80.000	GNDILLU
63	46.000	3527.000	80.000	80.000	VDDILLU5V
64	46.000	3287.000	80.000	80.000	VDDEYESENSE1
65	46.000	3047.000	80.000	80.000	VDDEYESENSE2
66	46.000	2923.000	80.000	80.000	EN_ILLU
67	46.000	2803.000	80.000	80.000	EN_ILLU_N_5V
68	46.000	2426.000	80.000	80.000	EFUSE
69	46.000	2251.000	80.000	80.000	VDDD1V8
70	46.000	2125.000	80.000	80.000	VDDD1V5
71	46.000	1913.000	80.000	80.000	GNDD
72	46.000	1715.000	80.000	80.000	GND A
73	46.000	1540.000	80.000	80.000	VDDA3V3
74	46.000	1365.000	80.000	80.000	GND A
75	46.000	1200.000	80.000	80.000	VDDA1V5
76	46.000	925.600	80.000	80.000	CSICN

**(table continues...)**

**2 Bare Die, Pads, CRA and Assembly**
**Table 2 (continued) Pad Coordinates**

Pad no	X [ $\mu\text{m}$ ]	Y [ $\mu\text{m}$ ]	dX [ $\mu\text{m}$ ]	dY [ $\mu\text{m}$ ]	Pad name
77	46.000	805.600	80.000	80.000	CSICP
78	46.000	618.400	80.000	80.000	CSID0N
79	46.000	498.400	80.000	80.000	CSID0P
80	46.000	311.200	80.000	80.000	CSID1N
81	46.000	191.200	80.000	80.000	CSID1P

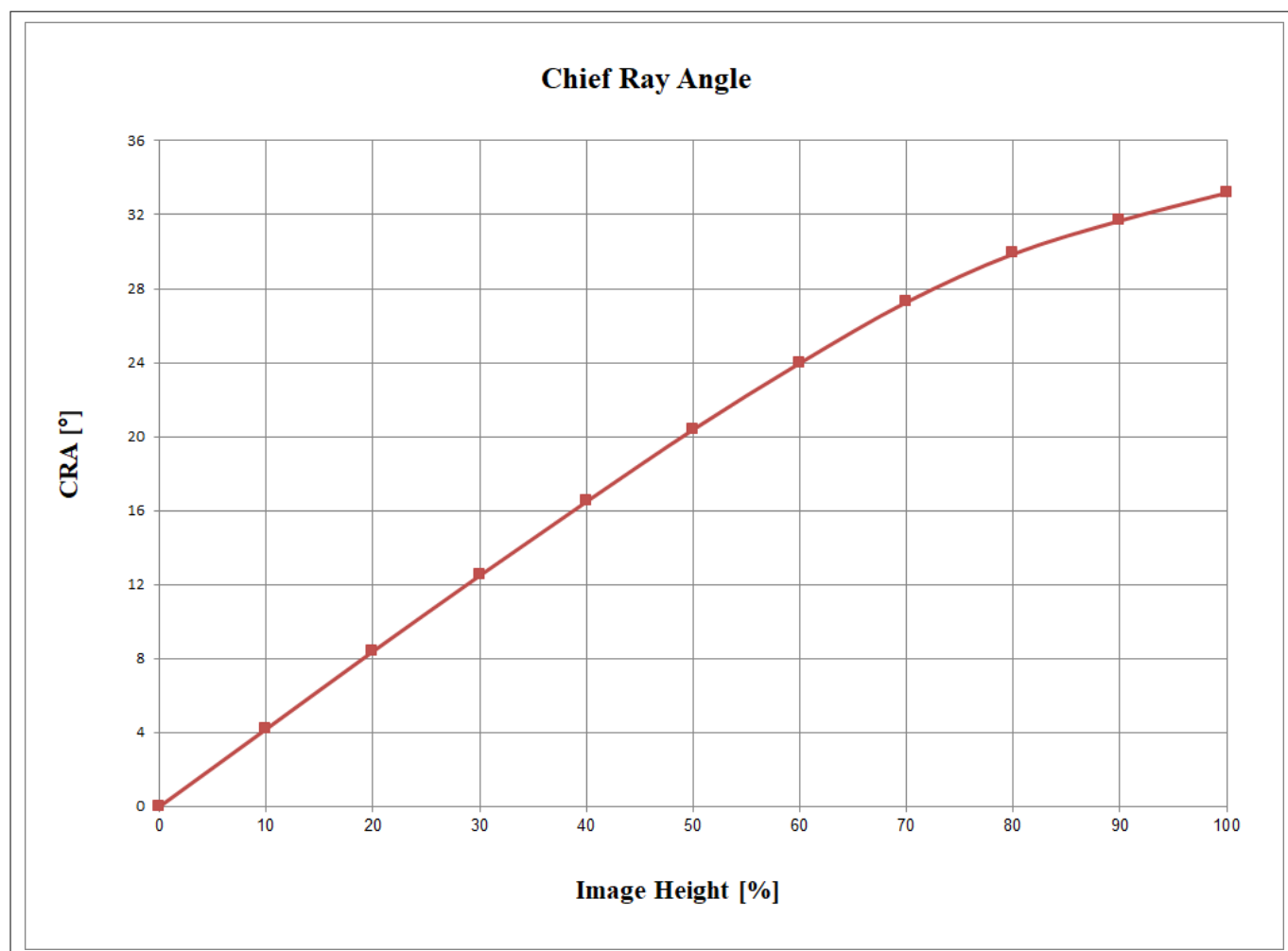
**2.3 CRA characteristics of recommended lens**

Table 3 and Figure 5 show the CRA(chief ray angle) of the IRS2975C sensor.

**Table 3 CRA**

Field [%]	Image Height [mm]	CRA [°]
0	0.000	0
10	0.150	4.2
20	0.300	8.4
30	0.450	12.5
40	0.600	16.5
50	0.750	20.4
60	0.900	24
70	1.050	27.3
80	1.200	29.9
90	1.350	31.7
100	1.500	33.2

## 2 Bare Die, Pads, CRA and Assembly



**Figure 5** CRA

## 2.4 Assembly information

### Die Attach

Best performance is achieved if the die is attached to the PCB using conductive glue and connecting the die attach area to ground potential. However, this is only a recommendation and using non-conductive epoxy glue has also been shown to be acceptable.

### Wire Bonding

For printed circuit boards Infineon uses a plasma cleaning process before wire bonding to avoid delamination of mold compound to solder resist interface. This also results in improved and long term reliable wire bond quality. [Table 4](#) defines the recommendations for wire bonding. The recommended wire bonding technology is thermo sonic ball-wedge bonding.

**Table 4** Bonding Information

Parameter	Values			Unit	Note or test condition
	Min.	Typ.	Max.		
Passivation Opening		80		μm	
Wire Diameter		25		μm	

(table continues...)

### 3 Reference schematic

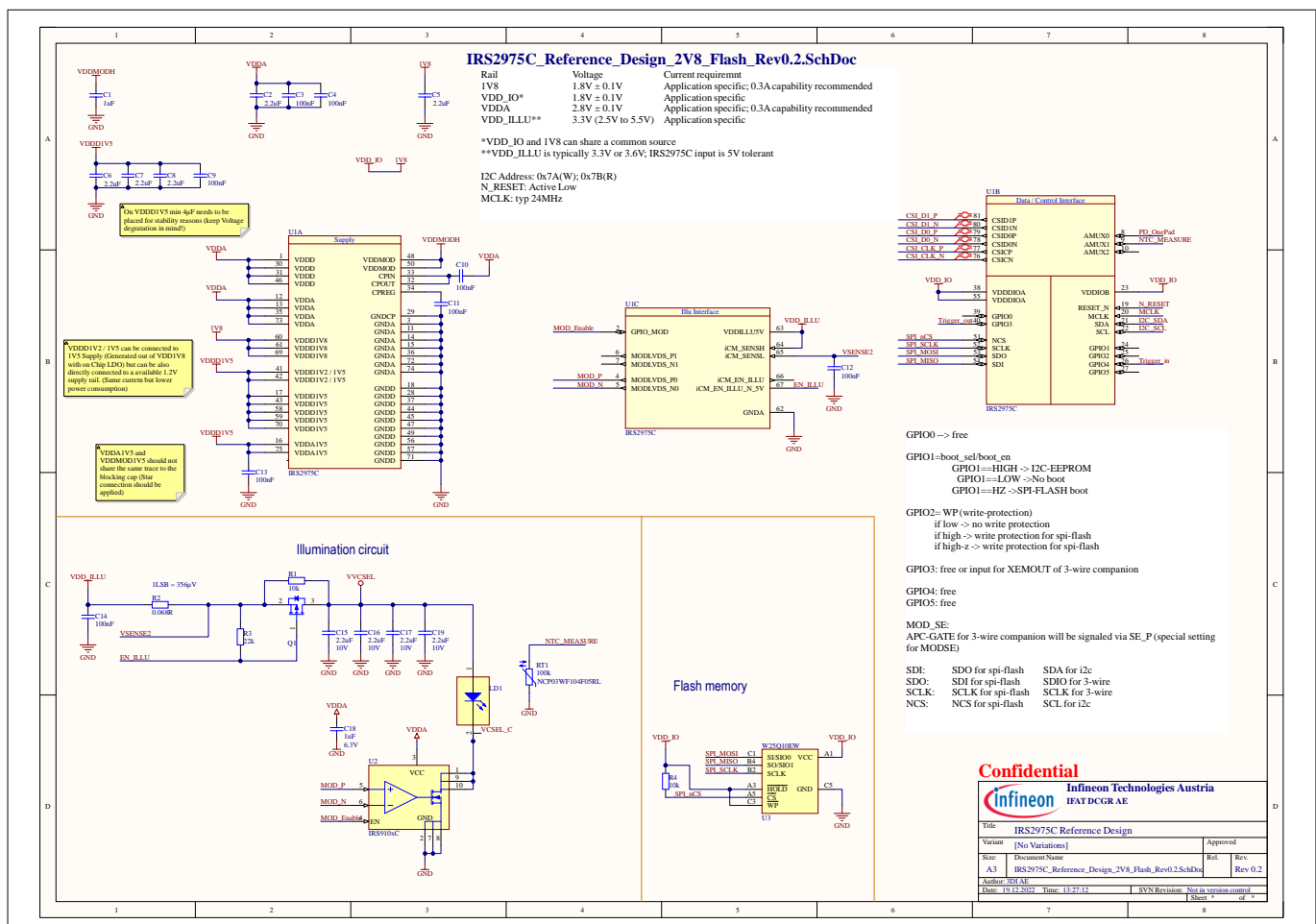
**Table 4 (continued) Bonding Information**

Parameter	Values			Unit	Note or test condition
	Min.	Typ.	Max.		
Wire Material		Au			
Ball Diameter	55	60	65	μm	
Ball Height	9	13	17	μm	
Shear Strength		15		cN	
Pull Strength		3		cN	
Bonding Temperature		150		°C	Measured on chip surface

## 3 Reference schematic

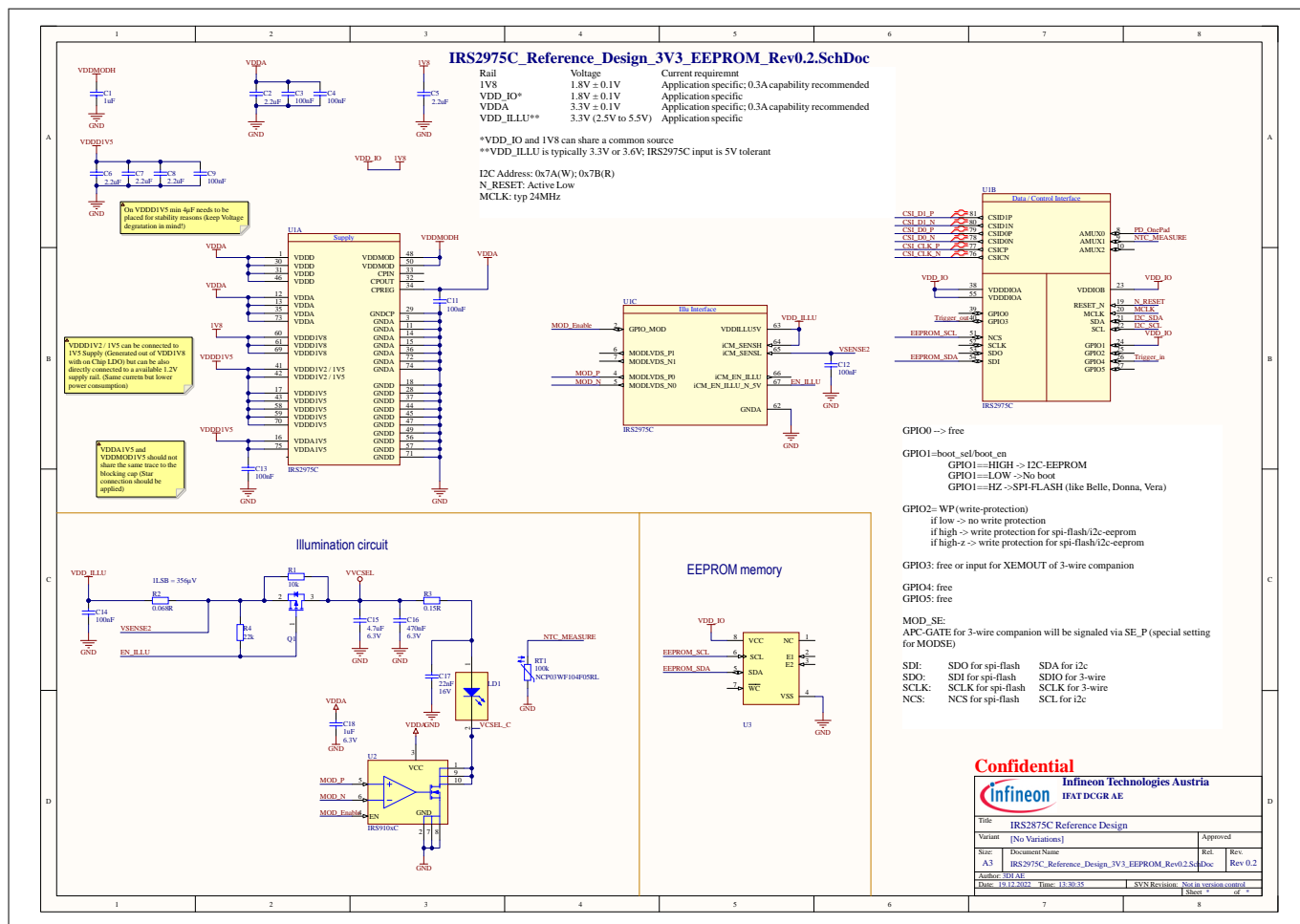
The following figures show the IRS2975C schematics for the available sensor power supply options with either 2.8V main supply voltage (see Figure 6), or 3.3V main supply voltage (see Figure 7) respectively.

The schematics show the sensor schematic symbol which is divided into the data/control interfaces, the illumination interface, as well as the power supply, that shows the corresponding sensor supply domains together with the required blocking capacitors. The illumination circuit incorporating the IRS910xC VCSEL driver is connected to the sensor's LVDS output and the corresponding GPIO for the modulation enable signal.



**Figure 6 Reference schematic IRS2975C with 2.8V Supply and Flash Memory**

### 3 Reference schematic



**Figure 7 Reference schematic IRS2975C with 3.3V Supply and EEPROM Memory**

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**4 Functional description****4 Functional description**

This section will give an overview of the IRS2975C functionality and measurement principle.

The IRS2975C is enabling a continuous wave (CW) time of flight measurement method which can be enhanced by using coded light modulation and suppression of background light (SBI) within each pixel. The CW method requires to expose the pixel to the modulated light reflected by an object which is accumulating the generated electron-hole pairs on both of the two nodes of the pixel. For a typical CW ToF depth frame, 4 raw data measurements need to be done to be able to map the measured phase to the appropriate distance.

The IRS2975C implements a standard MIPI CSI2 interface including the camera control interface. The raw data are transferred to the application controller using the high speed MIPI interface. As the one complete Z-frame consists of minimum 4 individual raw data frames the IRS2975C can combine the 4 raw (if the z-frame contains higher amount of raw frames is also supported) into a single MIPI frame and therefore improving heavily the processing load within the low level driver of the application processor (AP).

The sensor supports a slave operation mode. In this scenario the sensor is triggered by a hardware signal from a master device (e.g. a RGB sensor or AP) to start the image capturing. To allow for several other synchronization methods (time stamping, illumination synchronization or enabling of power devices) a broad variety of GPIO signals are available.

As a ToF system always incorporates an active illumination which is typically realized as a vertical-cavity surface-emitting laser (VCSEL), several safety mechanisms are realized within the IRS2975C.

The IRS2975C provides the functionality to monitor the current through the VCSEL and switch-off the illumination if a too high current or unexpected behavior of the current is detected.

For CW based ToF the scene is illuminated with diffuse light which is normally generated using a optical diffuser. To maintain a safe function, the application need to make sure that the diffuser is still in place and not affected by mechanical stress or liquids inside the housing. IRS2975C provides several interfaces and functions to enable photo diode concepts for detecting the reflected light inside the housing of the illumination module, or transparent films like indium tin oxide (ITO) for detecting illumination module malfunctions.

VCSEL laser diodes usually do have a significant spread over production in optical output power and switching behavior. The IRS2975C supports a trimming procedure which can be performed during module production to compensate the VCSEL variations.

Within a ToF system the acquired depth data need to be compensated depending on module variations. The IRS2975C supports dedicated modes to reduce the calibration effort significantly. The acquired compensation values are typically stored on the module using an SPI flash which is directly supported by IRS2975C.

## 5 Electrical characteristics and parameters

### 5 Electrical characteristics and parameters

This chapter will give the main performance parameters, the absolute maximum ratings, all necessary interface parameters and the allowed operating conditions of the IRS2975C.

#### 5.1 Absolute Maximum Ratings

**Table 5 Absolute Maximum Ratings**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply Voltage at VDDILLU5V	V DDILLU5V	-0.5		6	V	
Supply Voltage at VDDA	V DDA	-0.5		4	V	
Supply Voltage at VDDx1V5	V DDx1V5	-0.3		1.7	V	
Supply Voltage at VDDD1V8		-0.5		4	V	
Supply Voltage at VDDMODL pins	V DDMODL	-0.3		1.7	V	
Supply Voltage at VDDDIOx	V DDDIOx	-0.5		4	V	
Maximum Input Voltage at GPIO, clock, reset, SCL, SDA, SCLK, NCS, SDI, SDO pins	V inIOmax	-0.3		V DDDIO + 0.3	V	
Maximum Input Voltage at DPHY Pins	V inDPHYmax	-0.3		V DDA1V5 + 0.3	V	
Maximum Input Voltage at AMUX and LVDS pins	V inAMUXmax	-0.3		VDDA + 0.3	V	
Maximum Input Voltage at VDDEYESENSE1, VDDEYESENSE2		-0.3		VDDILLU5V+0.3	V	
Maximum Current into GPIO, Clock, Reset, SCL, SDA, SCLK, NCS, SDO, SDI Pins	I IOmax			4	mA	
Maximum Current into Illumination Pins	I Illumax			4	mA	
Maximum Current into DPHY Pins	I DPHYmax			1	mA	
Maximum Current into AMUX and LVDS Pins	I LVDSmax			4	mA	
Maximum Current into EYESAFETY Output Pins EN_ILLU, EN_ILLU_N_5V				4	mA	
Bulk Temperature	T Bulk	-40		+125	°C	
Storage Temperature	T Storage	-40		+150	°C	
Thermal Resistance bare die	R th(ja)			2	K/W	Without glue, bare die
ESD Robustness HBM	ESD Class,HBM	ESD HBM Class 1C				According to JS-001 (<2kV)

(table continues...)

**5 Electrical characteristics and parameters**
**Table 5 (continued) Absolute Maximum Ratings**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
ESD Robustness CDM	ESD Class,CDM	ESD CDM Class C1				According to JS-002 (<500V); Stress performed in ceramic package C-FQFP-64
Latch Up	I LU	-100		100	mA	JEDEC JESD78

**5.2 Operation Conditions**
**Table 6 Electrical operation characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply Voltage at VDDx5V		2.5	3.3	5.5	V	
Supply Voltage at VDDA	V DDA3V3	3.1	3.3	3.5	V	
	V DDA2V8	2.6	2.8	2.95	V	
Supply Voltage at VDDx1V5 (if supplied externally without regulator)	V DDx1V5	1.4	1.5	1.6	V	
Supply Voltage at VDDD1V8	VDDD1V8	1.692	1.8	1.908	V	
Supply Voltage at VDDMODL Pins	VDDMODL		0		V	
Supply Voltage at VDDMODH Pins (if supplied externally without regulator)	VDDMODH	0.67	0.7	0.73	V	Depends on Voltage regulator setting, default: 0.7 V
Supply Voltage at VDDDIO	V DDDIO1V8	1.692	1.8	1.908	V	
Supply Voltage at VDDSEIO	V DDSEIO	3.1	3.3	3.5	V	
Supply Ramp Time to VDDmax (except VDDILLU5V if larger than 3.6V)		2			µs	
Supply Ramp Time for VDDILLU5V > 3.6V				1	V/µs	
Delta Supply Voltage between two VDDx1V5 Pins	ΔV DDx1V5			50	mV	
Delta Supply Voltage between two VDDA Pins	ΔV DDx1V5			50	mV	
Current Consumption Active VDDx5V			860	960	µA	

**(table continues...)**



**5 Electrical characteristics and parameters**
**Table 6 (continued) Electrical operation characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Current Consumption Capturing VDDA			75	85	mA	@100 MHz modulation frequency
Current Consumption Capturing VDDD1V8 + VDDDIO @ 100 MHz			82	90	mA	@100 MHz modulation frequency
Current Consumption Readout VDDA			50	55	mA	2 Lane operation
Current Consumption Readout VDDD1V8 + VDDDIO			85	100	mA	2 Lane operation
Current Consumption IDLE VDDx5V			280	430	μA	
Current Consumption Idle VDDA			0.5	1.3	mA	low power state between z-Frames, CSI-2 is in low power mode
Current Consumption Idle VDDD1V8 + VDDDIO			5.5	8	mA	low power state between z-Frames, CSI-2 is in low power mode, eye safety running
Current Consumption Power Down VDDx5V				310	μA	
Current Consumption Power Down VDDA	I PWD_3V3			400	μA	
Current Consumption Power Down VDDD1V8 + VDDDIO				50	μA	
Current Dependency Ambient Light	I AMBIENT			2.5	μA/(W/m <sup>2</sup> )	DC Light 940nm , in power down, measured on VDDA3V3
Modulation Frequency	f Mod_LVDS	10		200	MHz	LVDS Interface
Bulk Temperature	T Bulk	-20		85	°C	
Reference Frequency	f ref	10	24	35	MHz	
Ref clock Jitter	ref jitter			10	ps	
Ref clock duty cycle	ref DC	40	50	60	%	

**5 Electrical characteristics and parameters**
**5.3 Pixel / Sensor Characteristics**
**Table 7 Pixel / Sensor characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Imager Resolution X Visible	Rx		240		pixel	Visible Pixels
Imager Resolution X Dark	Rx_dark		0		pixel	Dark Pixels
Imager Resolution X Active	Rx_active		240		pixel	Electrically active Pixels
Imager Resolution Y Visible	Ry		180		pixel	Visible Pixels
Imager Resolution Y Dark	Ry_dark		2		pixel	Dark Pixels (combination of dark / $\mu$ Lens / no $\mu$ Lens)
Imager Resolution Y Active	Ry_active		182		pixel	Electrically active Pixels
Number of defect pixel clusters $\geq 1 \times 2$	Rfail_cluster			0	pixel	cluster $\geq 1 \times 2$ not allowed, Cluster is horizontal, vertical, and diagonal
Number of Defect Pixels				40	pixel	
Pixel Pitch x	PPx		10		$\mu\text{m}$	
Pixel Pitch y	PPy		10		$\mu\text{m}$	
Integration Time	tINT	0.01		20.97	ms	@100MHz modulation, scales linearly (14 bit counter with max 7 bit prescaler)
Average Noise Floor	Nreset_mean		4	5	LSB	average of array; standard deviation over time; contains Reset, ReadOut, kTC and ADC noise
Standard Deviation Noise Floor	Nreset_sigma			1.5	LSB	
Average Effective Conversion Capacitance	Cdiode		6.7		fF	Consists of Diode, Wiring + Hold Transistor; readout gain not considered
Average Full-Scale-Pixel-Output-Voltage-Swing, 25°C	FS25	500	620		mV	25°C

**(table continues...)**

**5 Electrical characteristics and parameters**
**Table 7 (continued) Pixel / Sensor characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Average Full-Scale-Pixel-Output-Voltage-Swing, 85°C	FS85	350	480		mV	85°C
Fixed-Pattern Phase Noise	FPPN			4	cm	standard deviation, f=80MHz
Dark Slope Differential (mean value), 25°C	Slopedark_diff_mean_25C	-1		1	mV/m s	25°C, at ADC-input
Dark Slope Differential (1 Sigma), 25°C	Slopedark_diff_sigma_25C			1	mV/m s	25°C, at ADC-input
Dark Slope Differential (mean value), 85°C	Slopedark_diff_mean_85C	-4		4	mV/m s	85°C, at ADC-input
Dark Slope Differential (1 Sigma), 85°C	Slopedark_diff_sigma_85C			4	mV/m s	85°C, at ADC-input
Optical Wavelength	$\lambda$		940		nm	
Sensitivity Mean	Smean	29	36		mV/m s/pW	25°C to 85°C, Pixel Sensitivity measured at ADC Input
Sensitivity 1 Sigma	Ssigma		2	4	mV/m s/pW	25°C to 85°C
Contrast (Demodulation Efficiency) mean value, DC	DCCmean	65	77		%	fmod = DC
Contrast (Demodulation Efficiency) 1 sigma, DC	DCCsigma			4	%	fmod = DC
Contrast (Demodulation Efficiency) mean value, 80 MHz	ACCmean_80MHz	58	72		%	fmod = 80 MHz
Contrast (Demodulation Efficiency) 1 sigma, 80 MHz	ACCsigma_80MHz			4	%	fmod = 80 MHz
Average Signal-to-Noise-Ratio per light energy, 25°C	SNRmean_25C_kTC	15.9	19.3		1/(ms*pW)	25°C, Sensitivity * Contrast (80MHz) / Noise Floor (mV), not photon-shot-noise limited
Standard Deviation Signal-to-Noise-Ratio per light energy, 25°C	SNRsigma_25C_kTC		4		1/(ms*pW)	25°C
Average Signal-to-Noise-Ratio per light energy, 85°C	SNRmean_85C_kTC	15.9	19.3		1/(ms*pW)	85°C, Sensitivity * Contrast (80MHz) / Noise Floor (mV), not photon-shot-noise limited

**(table continues...)**

**5 Electrical characteristics and parameters**
**Table 7 (continued) Pixel / Sensor characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Standard Deviation Signal-to-Noise-Ratio per light energy, 85°C	SNRsigma_85C_kTC		4		1/(ms*pW)	85°C
Pixel Responsivity; Mean of all Pixels per Die		0.18	0.23		A/W	25°C to 85°C Temperature Range, 940 nm, Technology Responsivity = Pixel Responsivity (this value) / (Fill Factor with $\mu$ Lens), measurement: CRA corrected Photo Current / (light power in $[W/m^2] * 10\mu m * 10\mu m$ ), No fillfactor

**5.4 Illumination Output Characteristics**
**Table 8 Illumination output characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
LVDS Output Impedance, Single-Ended	Z OUT,SE	40		140	$\Omega$	@ DC
LVDS Common Mode Output Voltage	V OS	1125		1275	mV	R LOAD,DIFF = 100 $\Omega \pm 1\%$
LVDS Differential Output Voltage	V OD	250		400	mV	R LOAD,DIFF = 100 $\Omega \pm 1\%$

**5 Electrical characteristics and parameters**
**5.5 Illumination Current Monitor Characteristics**
**Table 9 Illumination Current Monitor Characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Eye-Safety Start Up Time until Reset-Release				100	us	Time when applying VDDILLU5V until reset_n_eye_safety is released (start-up of 3.3V Regulators, Bandgap, 1.5V Regulator)
System gain error untrimmed		-10		10	%	nominal gain: 700mV/2048 = 342uV/LSB, mainly caused by ADC gain and reference voltage
System gain accuracy after trimming (temperature and voltage drift)		-2		2	%	The gain after trimming, nominal gain: 700mV/2048 = 342uV/LSB, mainly caused by ADC gain and reference voltage
Input Offset Voltage (with system chopper)		-1		1	LSB	
Single Ended Input Range VDDEYESENSE1 and VDDEYESENSE2 referred to VDDILLU5V		-1000		100	mV	Single Ended Input Range is VDDILLU5V-1V...VDDILLU5V+0.1V
Max. DC Sink Current of "Open-Drain" EN_ILLU_N_5V and EN_ILLU PAD				1	mA	
High Level Output Voltage of EN_ILLU PAD @ VDDILLU5V > 3.63V		3.0		3.63	V	no load current
High Level Output Voltage of EN_ILLU PAD @ 2.5V < VDDILLU5V < 3.63V		VDDILLU5V-0.5		VDDILLU5V	V	no load current
Low Level Output Voltage of EN_ILLU PAD		0		0.5	V	the "sink current" requirement should be used as load condition

**(table continues...)**

**5 Electrical characteristics and parameters**
**Table 9 (continued) Illumination Current Monitor Characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Low Level Output Voltage of EN_ILLU_N_5V PAD		0		0.5	V	max. sink current (see MIB-REQ-653) when VDDILLU5V=2.5V
Sampling Rate with nominal RC frequency			200		kHz	
Clock accuracy (Filter observation time accuracy, Sampling rate accuracy) without trimming		-25		25	%	
Clock accuracy (Filter observation time accuracy, Sampling rate accuracy) after trimming (temperature and voltage drift)		-6.5		6.5	%	variation due to temperature and supply; process trimmed;
Quantization step of programmable threshold for max. filter observation time			342		uV	
Maximum allowed differential Input Voltage				1	V	higher voltages damage the chip
R_pull_up C_load - Time Constant for EN_ILLU_N_5V PAD				8	µs	The external capacitive load along with the external pull up resistor determine the time constant for the pad. The pull up resistor is further more determined by the Max. Sink Current of "open-drain" EN_ILLU_N_5V PAD. Overall the time constant ensure that the pad read back feature is functional. The additional internal pull up resistor (1MOhm) fulfills if there is no bondwire connected to the pad.

**(table continues...)**

**5 Electrical characteristics and parameters**
**Table 9 (continued) Illumination Current Monitor Characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Capacitive load at eye-safety pad EN_ILLU PAD				100	pF	Given the maximum capacitive load, the pad readback feature has to be fully functional (88 RCO clock cycles delay allowed) There shall be no BoD event when PAD is loaded with max. Cap and switching

**5.6 D-PHY TX Electrical Characteristics**
**Table 10 D-PHY TX Electrical Characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Number of Data Lanes	#DLanes		2			
Number of Clock Lanes	#CLanes		1			
Data Rate per DPHY lane	DRDPHY			1000	Mbit/s	
D-PHY DDR clock speed	fDDR			500	MHz	
HS Transmit Static Common Mode Voltage	VCMTX	150	200	250	mV	
VCMTX Mismatch when Output is Differential-1 or Differential-0	ΔVCMTX(1,0)			5	mV	
HS Transmit Differential Voltage	VOD	140	200	270	mV	
VOD Mismatch when Output is Differential-1 or Differential-0	ΔVOD			10	mV	
HS Output High Voltage	VOHHS			360	mV	
Single-Ended Output Impedance (DC-Value)	ZOS	40	50	62.5	Ω	
Single-Ended Output Impedance Mismatch (Up/DOWN, P/N) (DC-Value)	ΔZOS			10	%	
Output Impedance of LP transmitter	ZOLP	110		300	Ω	

**(table continues...)**

**5 Electrical characteristics and parameters**
**Table 10 (continued) D-PHY TX Electrical Characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Exposure to exposure time for 2 MIPI lanes	$t_{ex2ex\_2MIPI}$			880	μs	
Data transmission time for 2MIPI lanes	$t_{data\_2MIPI}$			775	μs	

**5.7 I2C Interface Characteristics**
**Table 11 I2C Interface Characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
High Level Output Voltage	Vout_high_1V8	VDDDI O-0.5		VDDDI O	V	Iload=1mA, static driver capability
Low Level Output Voltage	Vout_low_1V8	0		500	mV	Iload=1mA, static driver capability
I2C Clock Frequency	fSCL			3.4	MHz	
Set-Up Time for a Repeated START condition	tSU_STA	160			ns	
Hold Time (repeated) START condition	tHD_STA	160			ns	
LOW Period of the SCL clock	tLOW	160			ns	
HIGH Period of the SCL clock	tHIGH	60			ns	
Data Set-Up Time	tSU_DAT	10			ns	
Data Hold Time	tHD_DAT	0		70	ns	
Rise Time of SCLH Signal	trCL			40	ns	
Rise Time of SCLH Signal after a Repeated START Condition and after an Acknowledge Bit	trCL1			80	ns	
Fall Time of SCLH Signal	tfCL			40	ns	
Rise Time of SDAH Signal	trDA			80	ns	
Fall Time of SDAH Signal	tfDA			80	ns	
Set-Up Time for STOP Condition	tSU_STO	160			ns	
SDA/SCL Pull-Up Resistor	RpullupI2C	1.15	1.5	2.3	kΩ	
Low Level Input Voltage	Vin_low	0		0.2*VDDIO	V	
High Level Input Voltage	Vin_high	0.8*VDDIO		VDDDI O+0.1	V	
Max. Leakage into SCL / SDA	IleakI2C			2	μA	



## 5 Electrical characteristics and parameters

### 5.8 SPI Interface Characteristics

**Table 12** Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
High Level Output Voltage	Vout_high	VDDDI O-0.5		VDDDI O	V	Iload=1mA, static driver capability; VDDIO supplied with 1.8V +5%
Low Level Output Voltage	Vout_low	0		0.5	V	Iload=1mA, static driver capability; VDDIO supplied with 1.8V +5%
Input Voltage Hysteresis SPI Pads		50			mV	@VDDDI O=1.8V, ATE: only tested for GPIO0 and SDA
High Level Input Voltage	Vin_high	0.8*V DDIO		VDDDI O+0.1	V	
Low Level Input Voltage	Vin_low	0		0.2*V DIO	V	
SPI data rate	f <sub>SPI</sub>		20		MHz	f <sub>sys</sub> = f <sub>ref</sub> = 24MHz\after PLL enable ; f <sub>sys</sub> = 160MHz

### 5.9 GPIOs & CLOCK PAD

**Table 13** Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
High Level Output Voltage Digital Pins (GPIOs & Clock Pad), VDDDI O = 1.8V	Vout_high	VDDDI O-0.5		VDDDI O	V	Iload=1mA, static driver capability
Low Level Output Voltage Digital Pins (GPIOs & Clock Pad), VDDDI O = 1.8V	Vout_low	0		0.5	V	Iload=1mA, static driver capability
Low Level Input Voltage Digital Pins (GPIOs & Clock Pad)	Vin_low	0		0.2*V DIO	V	
High Level Input Voltage Digital Pins (GPIOs & Clock Pad)	Vin_high	0.8*V DDIO		VDDDI O+0.1	V	
Capacitive Load for Digital Output Pins	CLoadGPIO			25	pF	operated @ 40 MHz
Pull Down Resistance	RpulldownGPIO	17.9	30	46.75	kΩ	

(table continues...)

## 5 Electrical characteristics and parameters

**Table 13 (continued) Electrical characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Pull Up Resistance	RpullupGPIO	22.5	30	55.2	kΩ	
Max. Leakage into GPIO or Clock Pad	ILeakGPIO			2	μA	

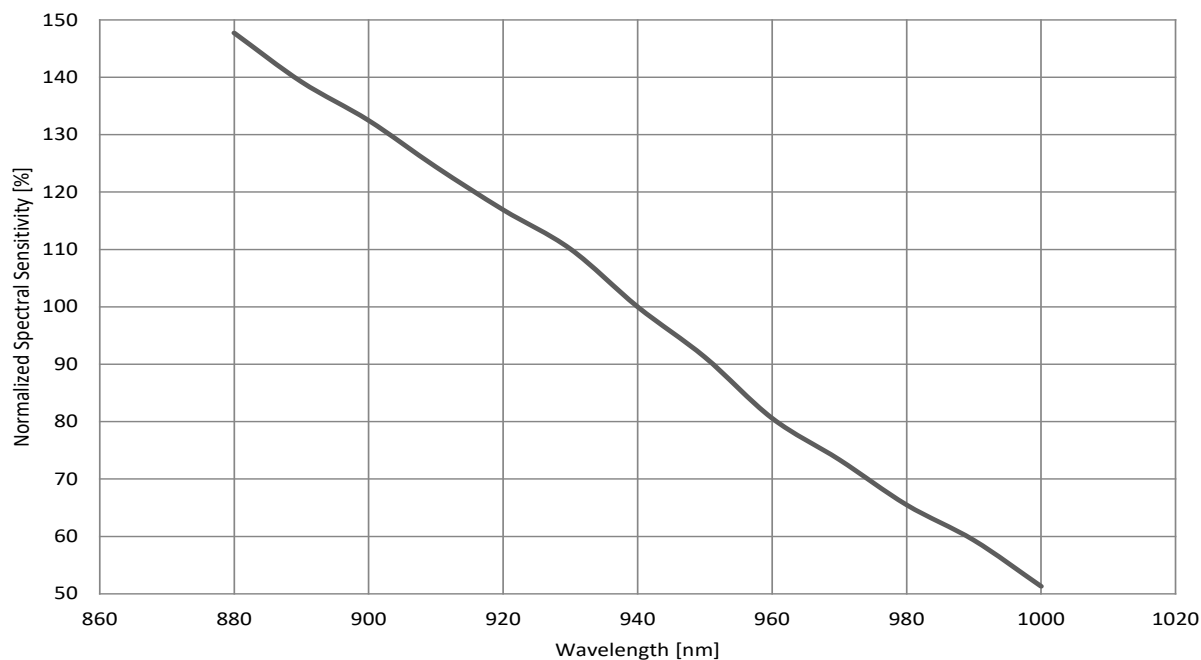
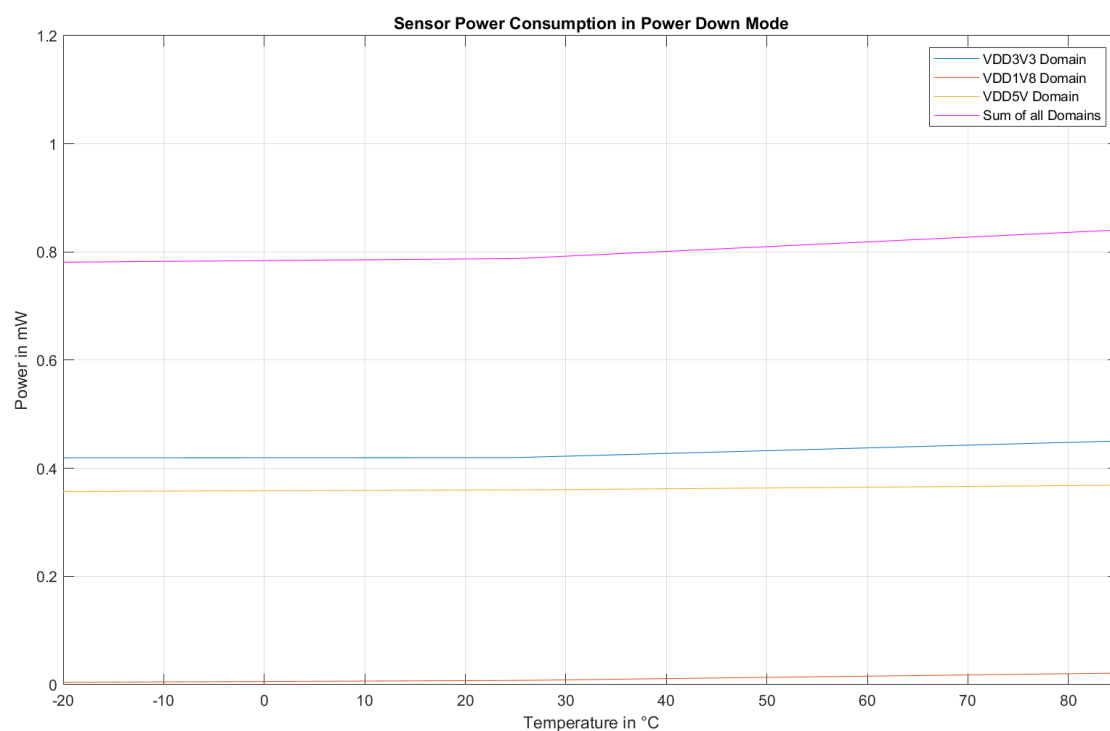
### 5.10 Brown-out and Start-up Characteristics

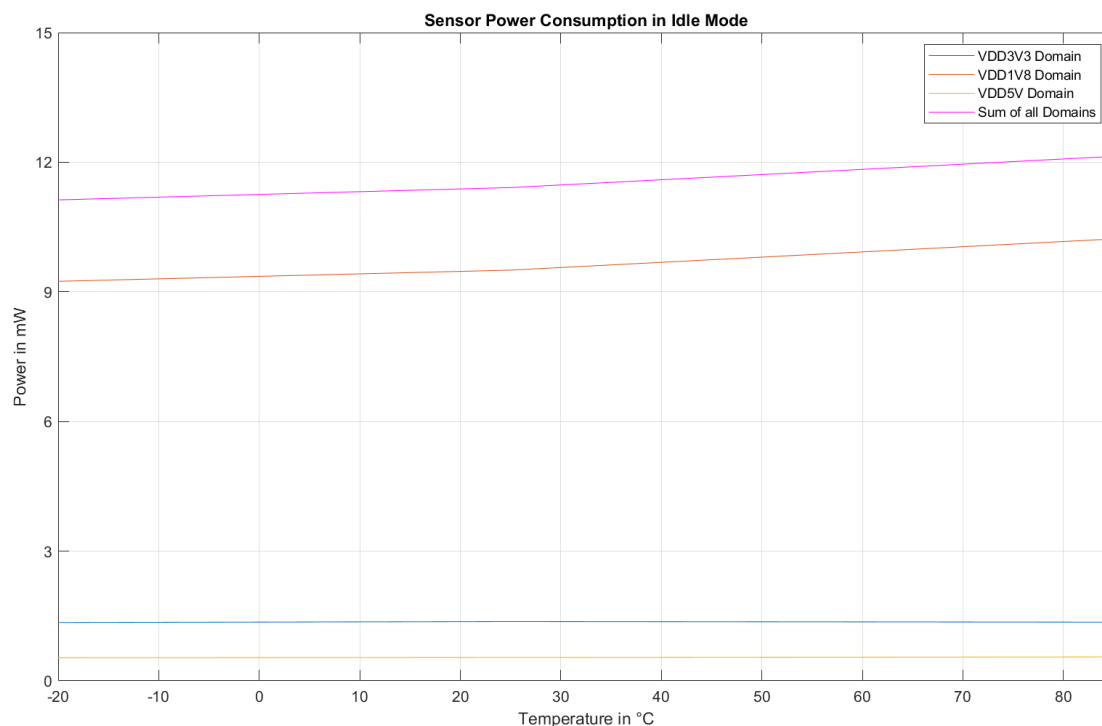
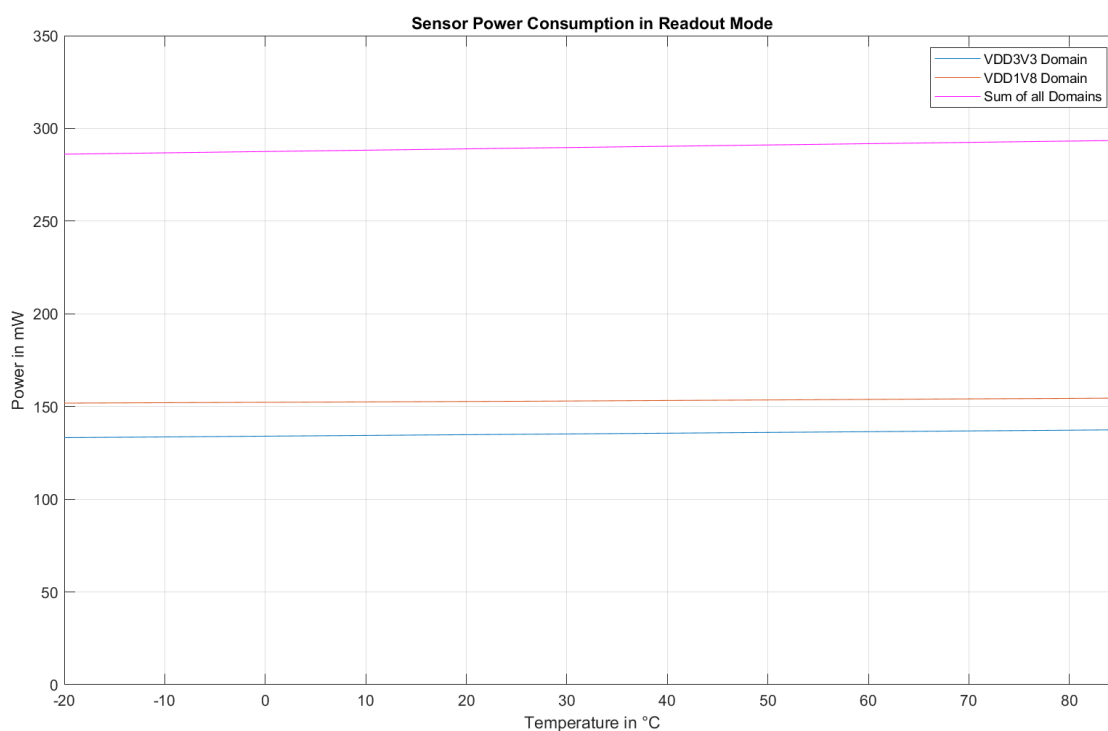
**Table 14 Electrical characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Brown-Out Threshold for VDDx1V5	V_BOx1V5	1.1	1.2	1.3	V	
Brown-Out Threshold for VDDD1V8	V_BO1V8	1.1	1.2	1.3	V	
Brown-Out Threshold for VDDDIO	V_BOIO	0.81	0.96	1.06	V	
Brown-Out Threshold for VDDA	V_BOA	2.14	2.24	2.34	V	
High Level Input Voltage Reset Pin	Vin_high	0.8*VDDIO		VDDIO+0.1	V	
Low Level Input Voltage Reset Pin	Vin_low	0		0.2*VDDIO	V	
Minimum Reset-Pulse Duration at RESET-Pin	treset	5			μs	Minimum time to detect reset (spike filter)
Startup Time to Idle	tstart_sleep			325	μs	fref=24MHz, reset release to Sleep mode

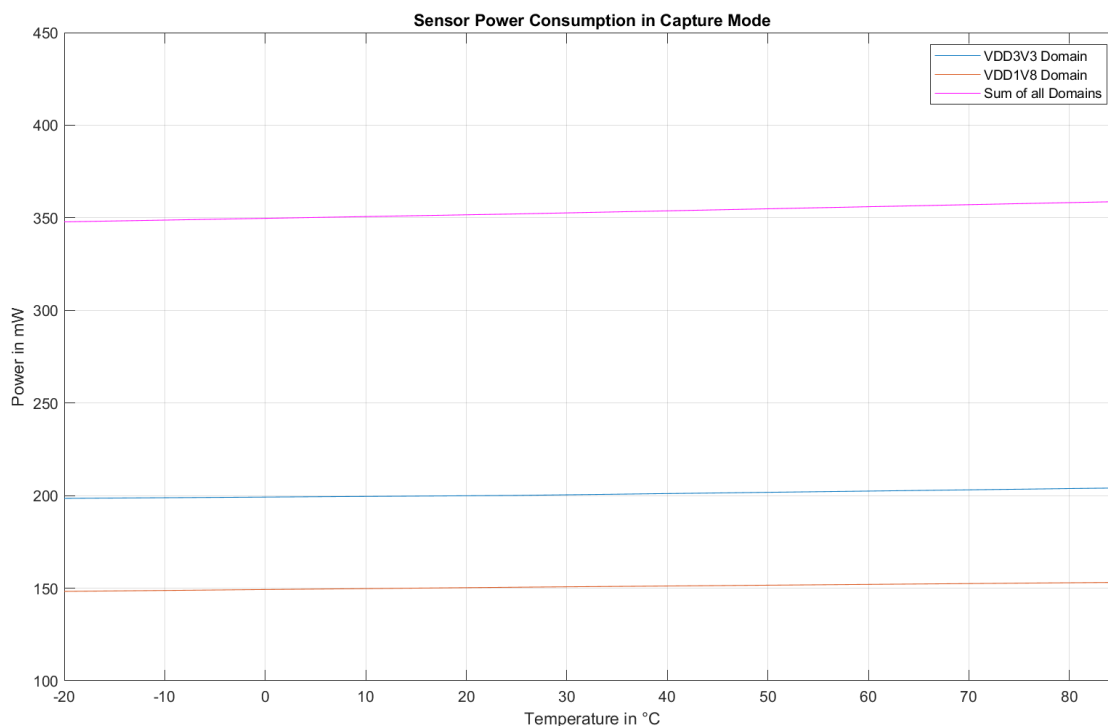
### 5.11 Typical performance characteristics

The following figures are representing the typical characteristics over various parameters which influencing the main performance of the sensor IRS2975C.

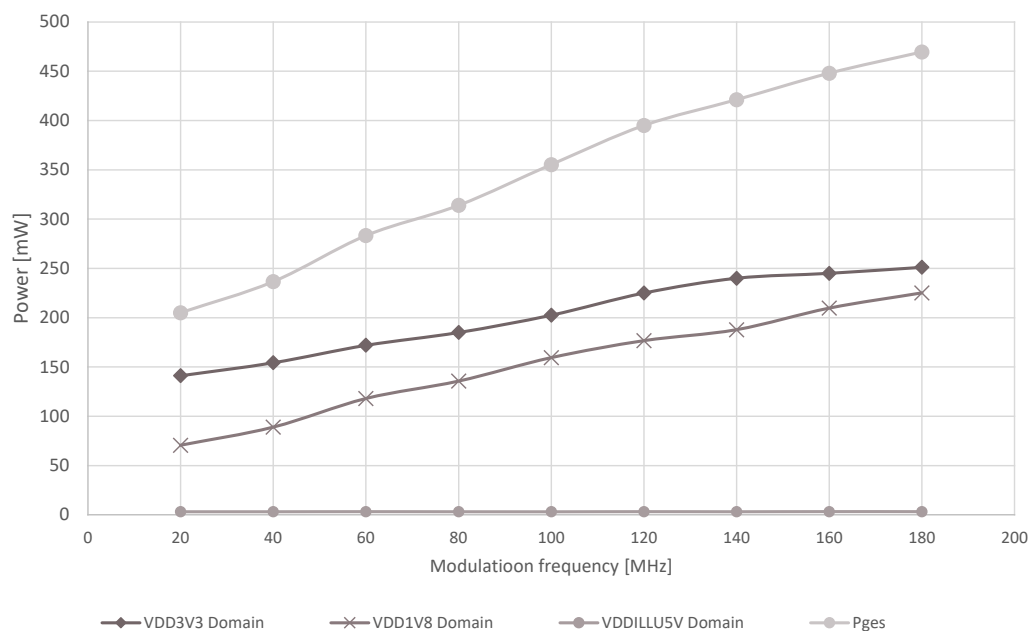
**5 Electrical characteristics and parameters****Figure 8** Typical normalized spectral sensitivity relative to 940 nm**Figure 9** Typical power consumption power down mode

**5 Electrical characteristics and parameters****Figure 10** Typical power consumption sleep mode**Figure 11** Typical power consumption conversion/Readout mode

## 5 Electrical characteristics and parameters

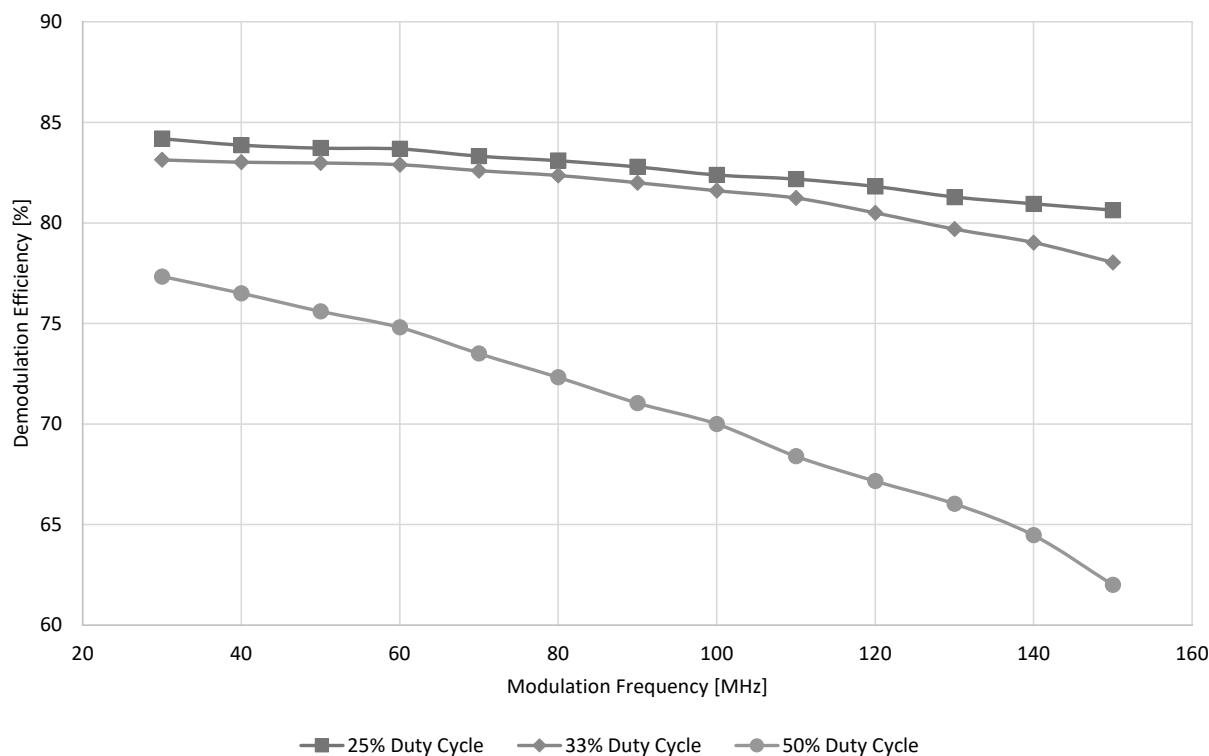


**Figure 12** Typical power consumption capture mode (Fmod = 100 MHz) vs temperature



**Figure 13** Typical power consumption capture mode vs. modulation frequency

## 6 RESET and Start-up



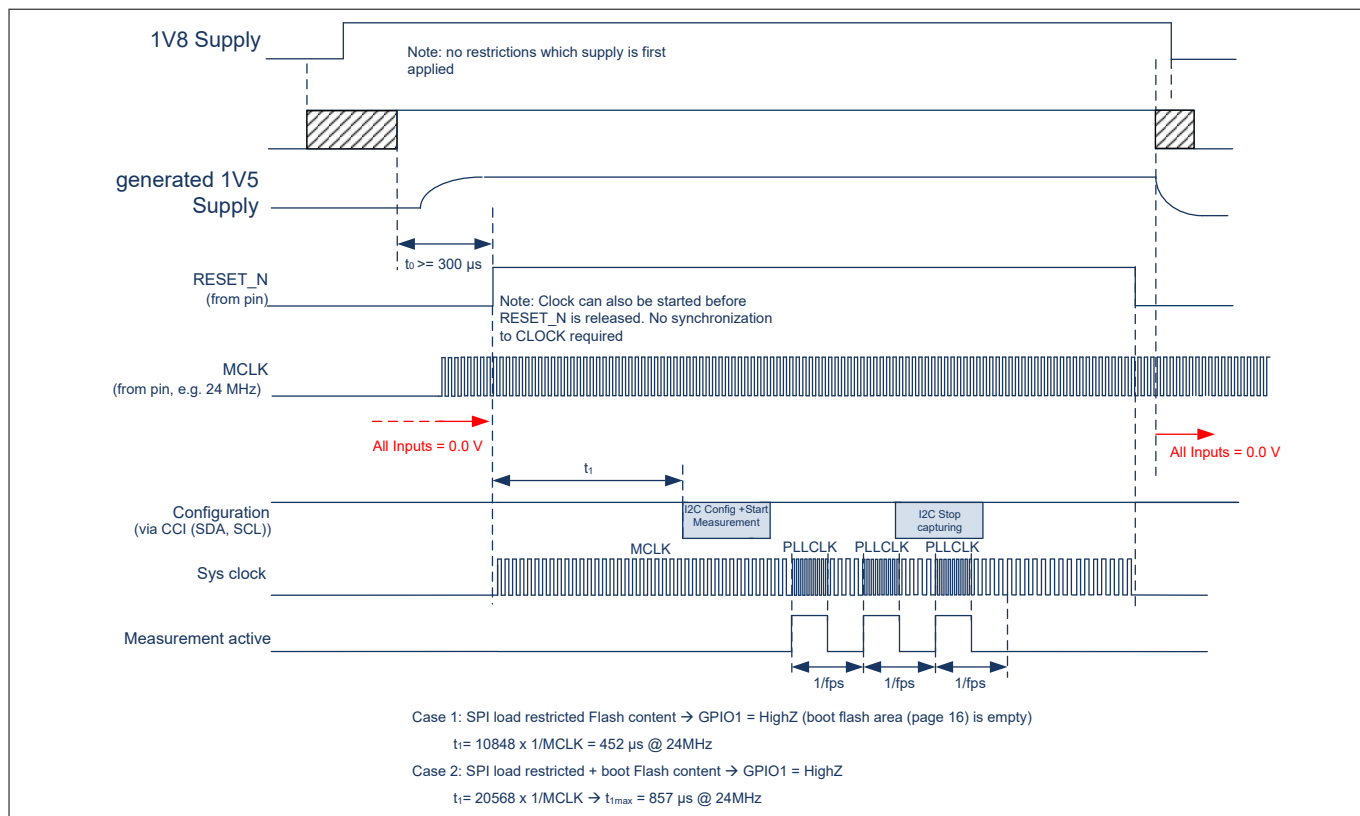
**Figure 14** Typical demodulation Efficiency vs. modulation frequency

## 6 RESET and Start-up

In general the IRS2975C does not require a dedicated supply enable order which enables a very easy handling from system perspective. The only requirement is that all pins need to be floating or low while the imager is not supplied. This maintains that the IRS2975C will not be supplied via the ESD protection circuits which may cause damage to the device.

The following timing diagram depicts the general start-up behavior of the IRS2975C.

## Revision history



**Figure 15 Start-up timing diagram**

A transition from high to low on the RESET\_N pin will set all registers back to default state. A transition from low to high will start the boot-loading process and enables all the relevant analog blocks.

To enable enhanced or customer specific functionality of the sensor the IRS2975C can load automatically additional functions from the attached flash through the SPI interface (EEPROM is usually too slow and small sized). The new function load is initiated automatically and will take additional time during the start-up procedure. Individual start-up timings for specific functions need to be determined case by case.

## Revision history

Document version	Date of release	Description of changes
Rev 0.1	2022-04-10	<ul style="list-style-type: none"> <li>initial target data sheet</li> </ul>
Rev 0.2	2022-05-16	<ul style="list-style-type: none"> <li>CRA image height values adopted</li> </ul>
Rev 1.0	2022-12-20	<ul style="list-style-type: none"> <li>added chapter Typical performance characteristics</li> </ul>
Rev 1.1	2024-02-13	<ul style="list-style-type: none"> <li>Extended physical dimensions table</li> <li>Re-structured Die information</li> <li>Corrected CRA table</li> <li>Added assembly information</li> </ul>

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**Edition 2024-02-13**

**Published by**

**Infineon Technologies AG**  
**81726 Munich, Germany**

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**Document reference**  
**IFX-sap1649148230923**

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